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Photonic Integration Trends

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Photonic Integration Technology Development

The assignment:

- Survey of available technology and its use or intended use,
  - technology trends and timeline (III-V, Silicon, others?),
  - key centers of existing research and sponsoring agencies
  - anticipated results in a geni 5-year time frame

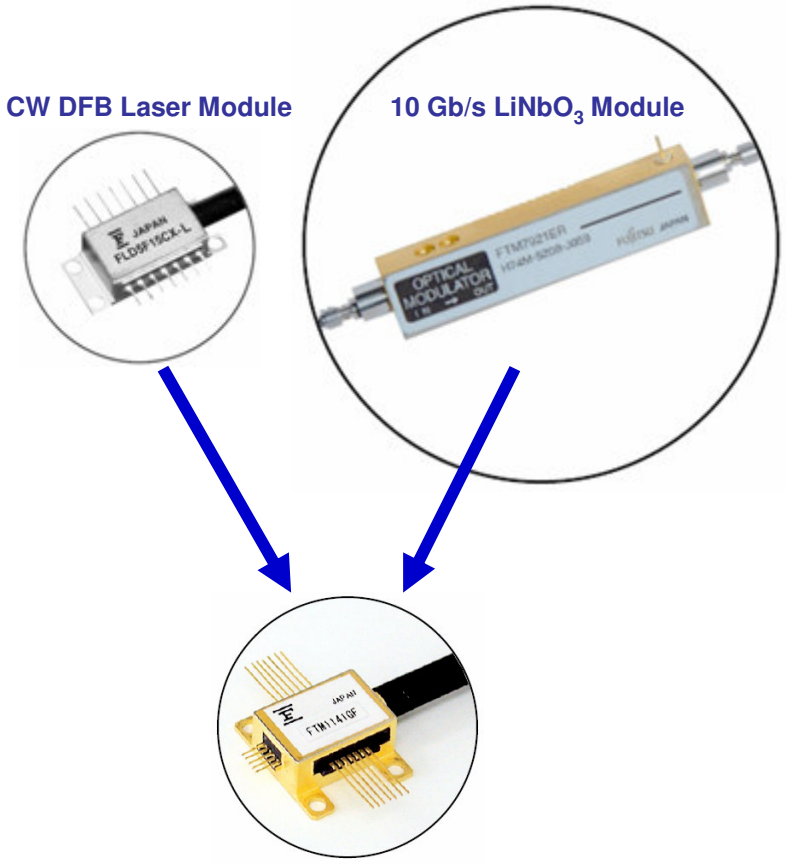
- Understand how GENI can be structured to take advantage of, and encourage, this important and rapidly developing technology.
  - Key subsystem functions with integration emphasis
  - Anticipated disruptive changes in cost or power
  - Candidates: optoelectronic transceiver technology, optical and or electro-optical processing, optical switching, RF/optical integration, and optical link and transport technologies.

What is the primary value proposition of photonic integration?

The photonic equivalent of a << 1¢ wire bond is two single mode alignments and two packages ($$$)

When two or more elements are optically interconnected to form a functional subsystem:

- we ***pay for*** two or more packages *(packaging can be 50-80% of cost, much more compelling than IC's)*
- we ***sacrifice reliability*** *(most failures are packaging related)*
- we get ***larger subsystems***; devices constrained to use long optical paths
- we ***lose power*** from fiber coupling efficiencies *(lower SNR)*
- we ***incur instabilities*** in coupling *(throughput, phase, reflections)*
- we ***lose*** wafer-level device ***uniformity***
- we have manufacturing ***inventory control issues***



10 Gb/s Integrated Modulator Laser Module Using InP-based PIC

Photonic Integration Technology Development

Technology choices:

- LiNbO3 & Polymers
  - Little integration for telecom; principally modulation
- InP
  - Only option offering full functionality, uncompromised materials
  - Most widely deployed with modest integration
  - Complex research underway for all-optical functionality
  - Recent deployments of higher-level integration in WDM transceivers, exploration of higher use of SOA's in network
- Si & Ge
  - All functions except source; high performance through high index contrast
  - Potential for lower cost structure; leverage ultra-precise fab technology
  - Integration with CMOS electronics

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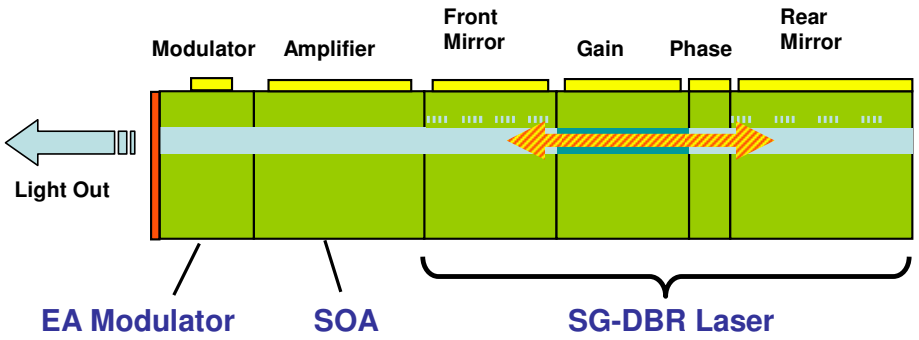
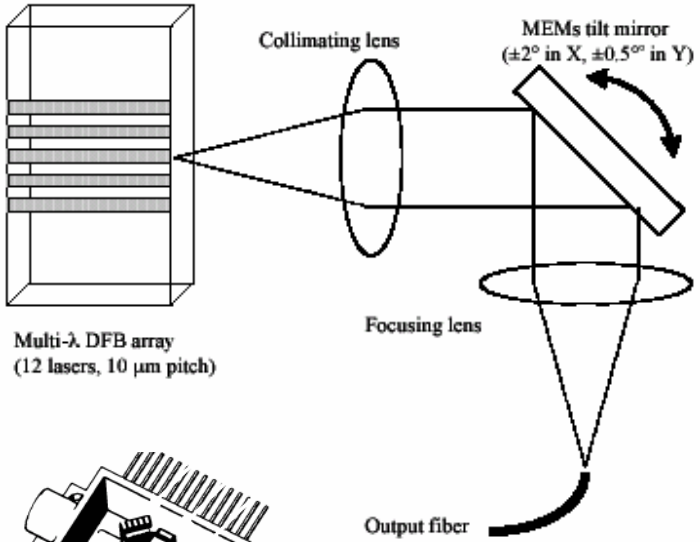
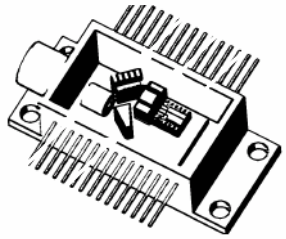
Photonic Integration Technology Development

Where are we today?

InP Integration Examples: Tunables



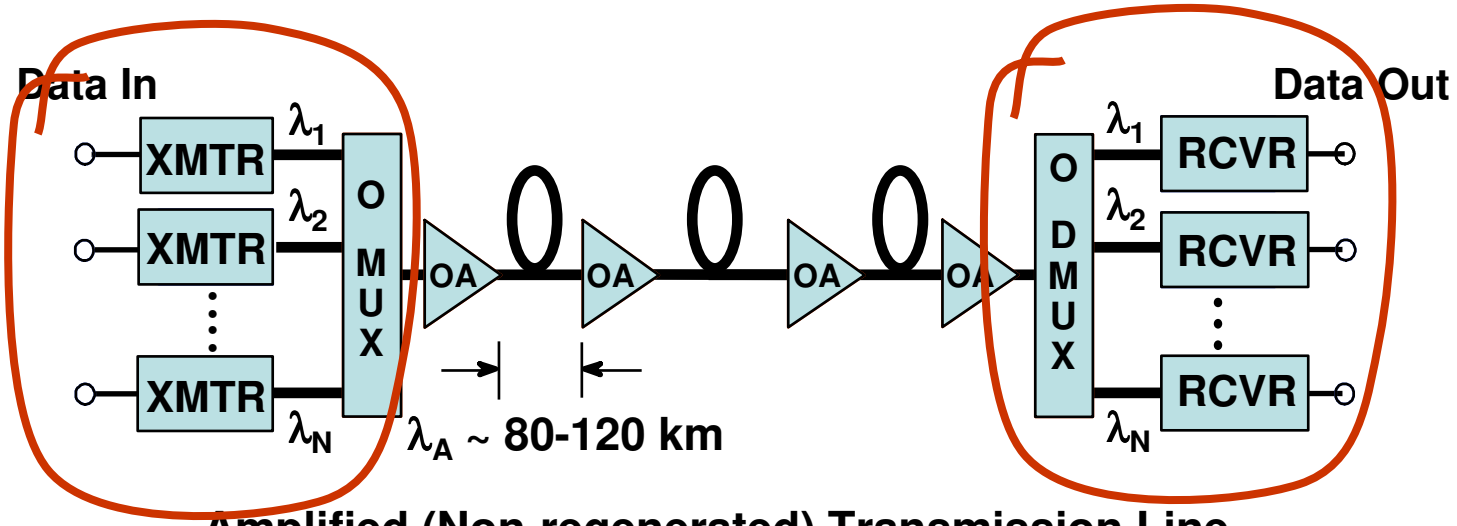




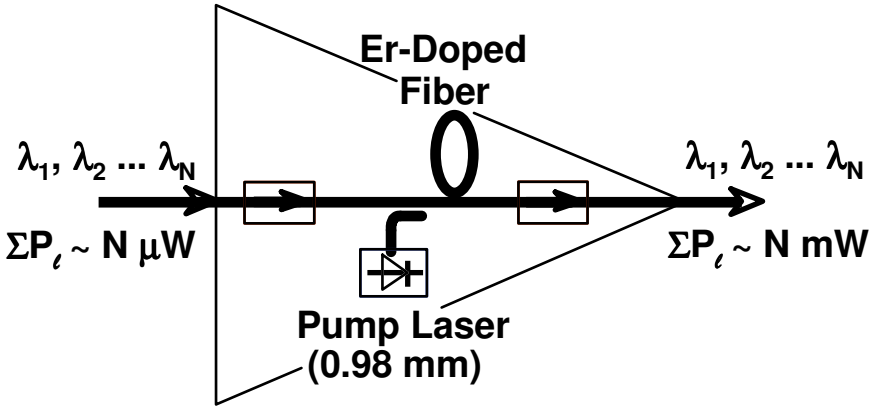
JDSU

Santur Corporation

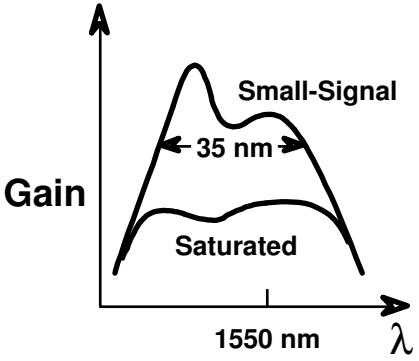
Optically Amplified WDM Transmission System



Amplified (Non-regenerated) Transmission Line



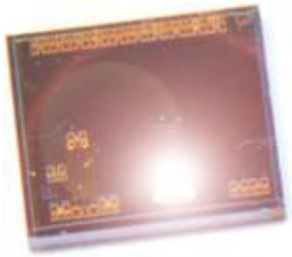
Erbium-Doped Fiber Amplifier



Gain Spectra

Large-Scale DWDM Photonic Integrated Circuits

100Gb/s Receive

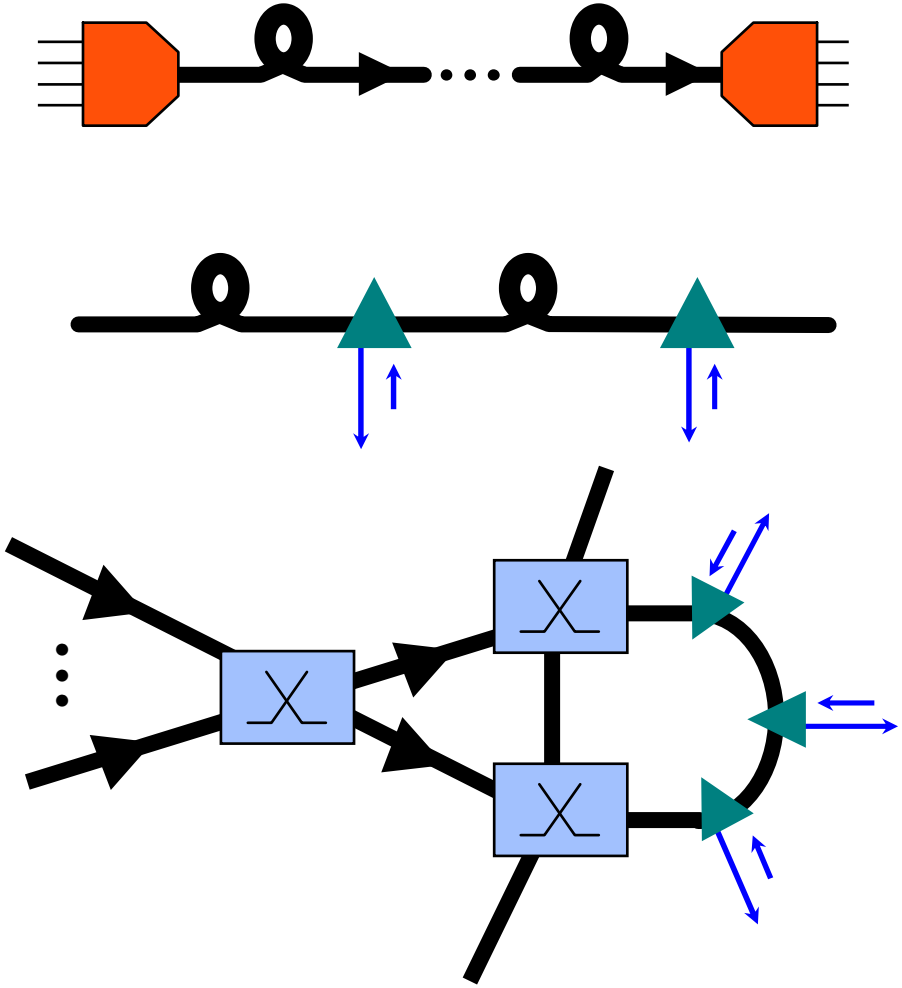


100Gb/s Transmit

- **Input: One fiber with 10 λ x 10 Gb/s ea.**
- **Output: 100 Gb/s electrical signals**
- **10 x 10Gb/s photodetectors**
- **Waveguides**
- **Optical demultiplexer**

- **Input: 100 Gb/s electrical signals**
- **Output: 10 λ x 10 Gb/s ea onto one fiber**
- **10 Tunable DFB lasers**
- **10 x 10Gb/s modulators**
- **Waveguides**
- **Optical multiplexer**
- **Power Monitoring / Flattening Control Elements**

infinera

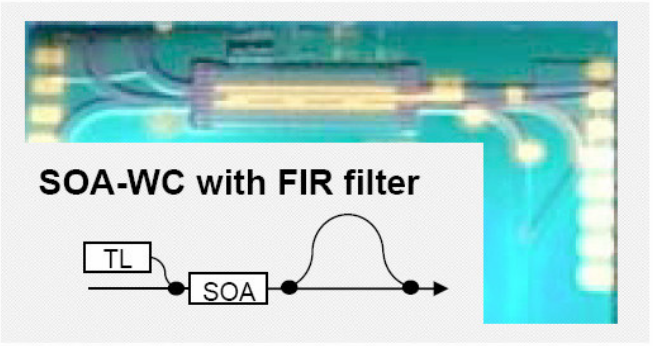


- **WDM/Point-to-Point Transport**
  - High Capacity Transmission
- **Fixed WDM/Multipoint Network**
  - Eliminate Conversion to Electronics for Add/Drop?
- **Photonic Cross-Connect**
  - All-Optical Network Flexible Re-configuration for Capacity
  - Network Self-Healing/Restoration
- ***Photonic Packet Switching?***

Wavelength Conversion at 40Gb/s

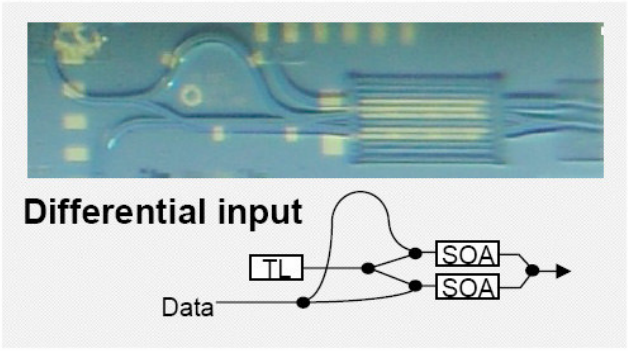
Two different approaches to wavelength conversion

- SOA + FIR filter
  - Single SOA but sensitive to output wavelength if operated in non-inverting mode



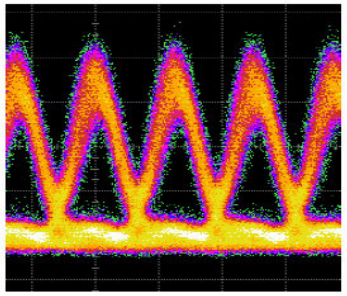
  - 3 ps input pulses
  - 3 - 5.5 dB penalty at BER = 10^{-9}

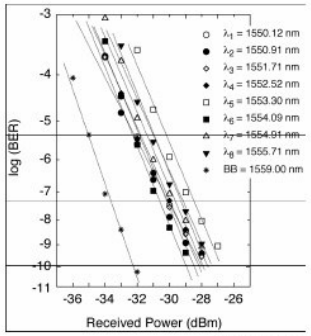
- MZI with differential input
  - Two SOAs but MZI works as wavelength filter for input and output not wavelength filtered

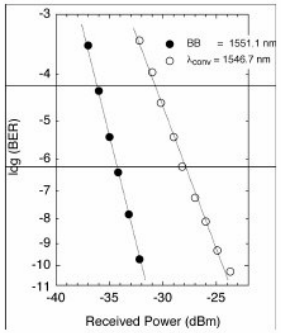


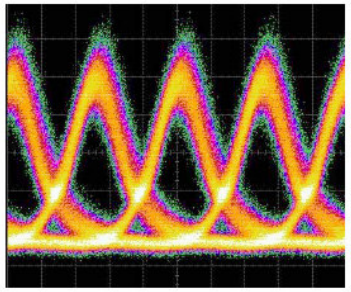
  - 8 ps input pulses
  - 6.5dB penalty at BER = 10^{-9}

Error-free wavelength conversion





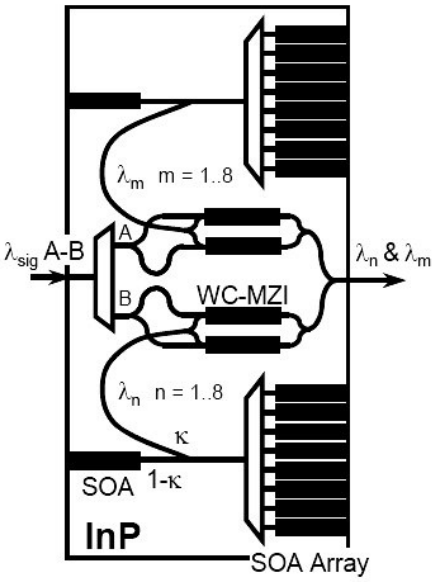


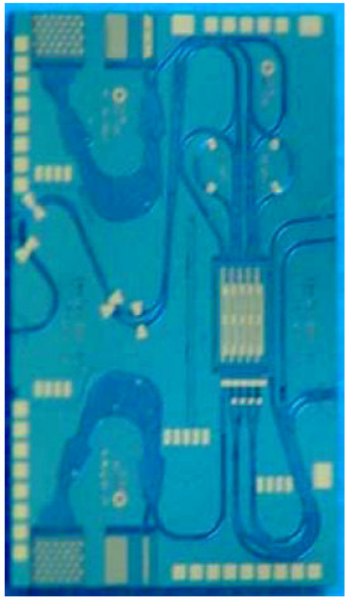


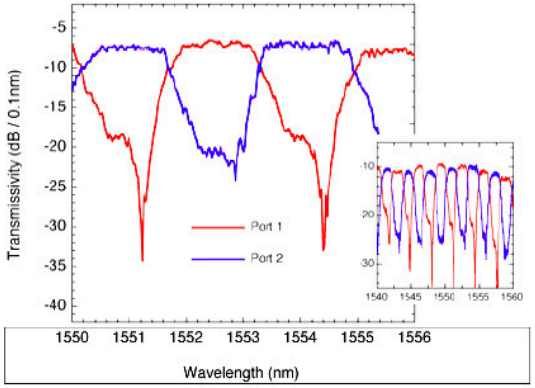
Lucent Technologies
Bell Labs Innovations

2x8 Wavelength Switch

- Monolithically Integrated 2x8-channel wavelength switch comprising
  - Two 8-channel MFLs
  - Two differential mach zender wavelength converters
  - 2-channel demux interleaver (first time ever in InP)
- MFL: channel spacing 100 GHz
  - operating currents: 80-95 mA
- Interleaver: 3-dB bandwidth ~180 GHz
  - insertion losses ~ 6-8 dB ER > 15 dB (not tuned)

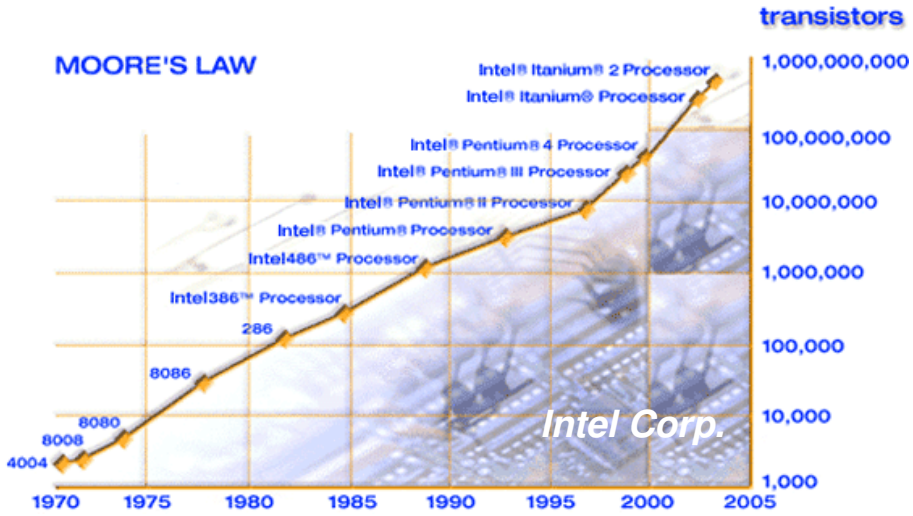


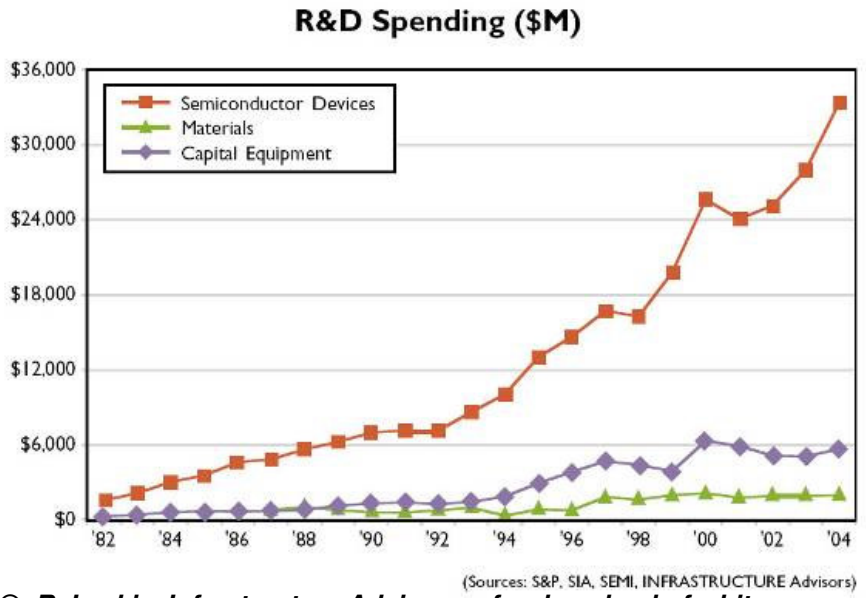




Why silicon photonics?

☞ ***Unprecedented process control platform that gives ever-increasing functionality per unit area at low cost***





© *R. Leckie, Infrastructure Advisors – for download of white paper, see http://www.infras-advisors.com/whitepaper.html*

- 1 Billion transistors onto a wafer at low cost?
  - → Extreme high yield processes, extreme predictability of results
- IC product development team project
  - → Done when tape-out complete!

CMOS IC Development – a world of difference from most of today's photonic chip design

The situation is not standing still!

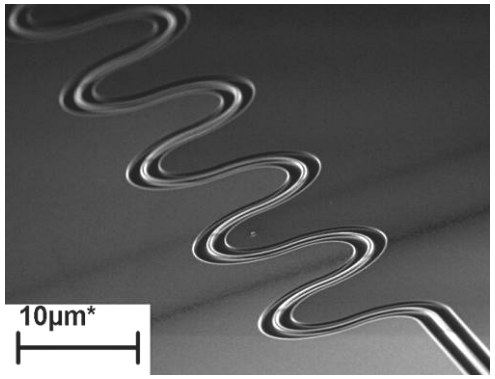
- In last 10 years alone:
  - – $300 Billion invested!
- Current run rate ('04):
  - – $41 Billion annually!
  - ~ 200,000 R&D staff!

Why Silicon Photonics?

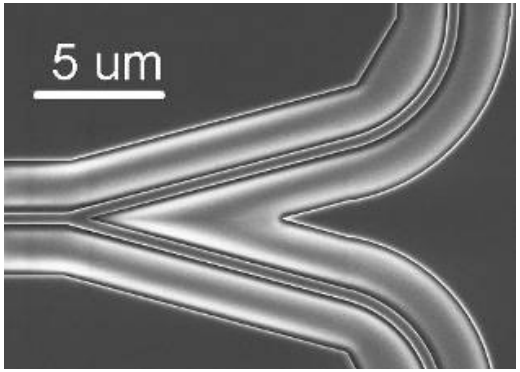
Performance Reasons:

- **Ultra-high index contrast**
  - **Low bending losses, compact devices**
  - **Benefits of TM polarization for some apps**
- ***High performance actives? Lower power devices?***
  - ***High confinement, small active volumes …?***
- **Potential for on-board integrated electronics**
  - **Low-cost, highly sophisticated CMOS drive, preamp, digital processing, …**
  - **Reduced parasitics, eliminate impedance matching issues …**

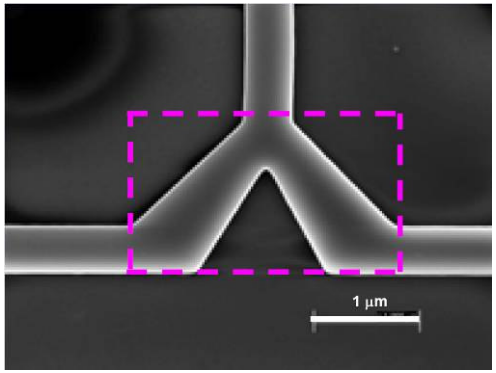
Benefits of Ultra-High Index Contrast: Ultra-Compact Structures



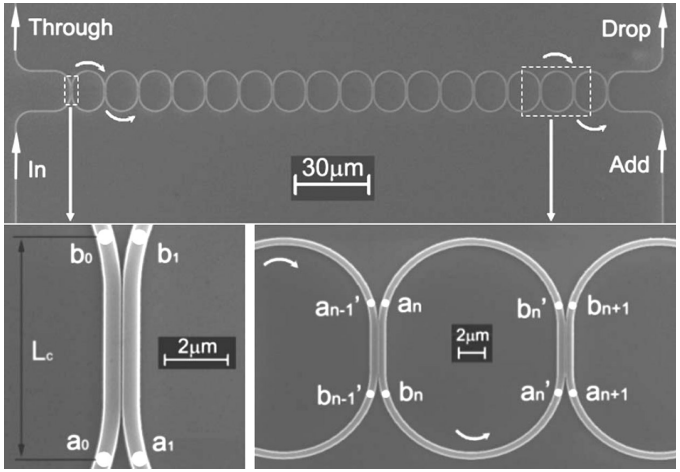
Example of losses for high-index-contrast "wire" waveguides: For 6.5 μm radius bends, losses are 0.0043 dB per 180º turn



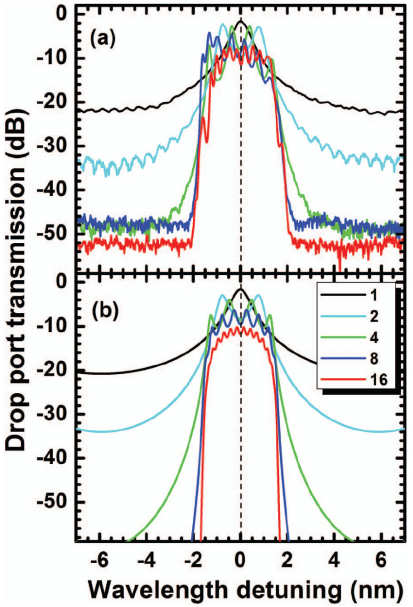
Adiabatic broadband splitter, 3 dB flat from 1450 to 1700nm



Resonant splitter, only 4μm² footprint!



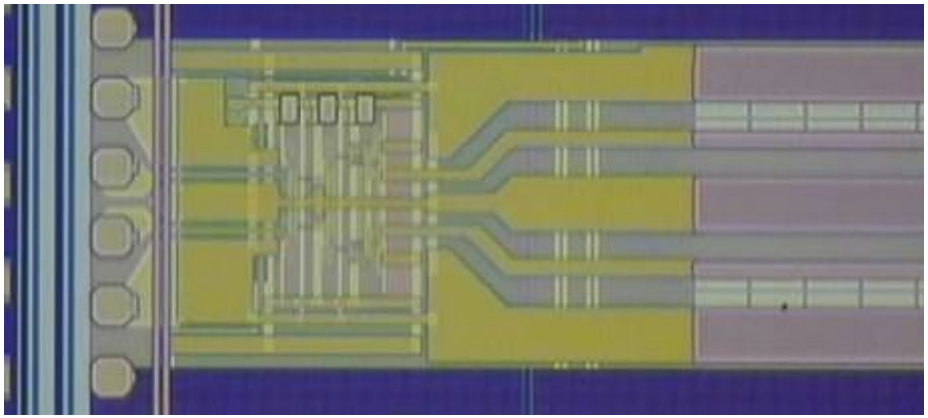
SEM view of cascaded ring add/drop filter



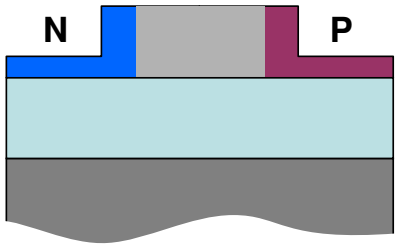
Experimental (top) and simulated (bottom) band-pass results for different numbers of rings

Vlasov, et al, IBM

CMOS Optical Mach-Zehnder Modulator



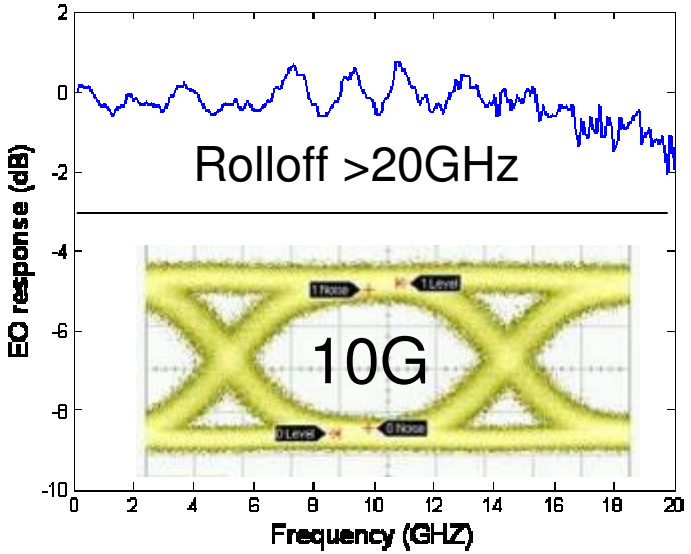
LUXTERA



Integration w/ Transistors is here now!

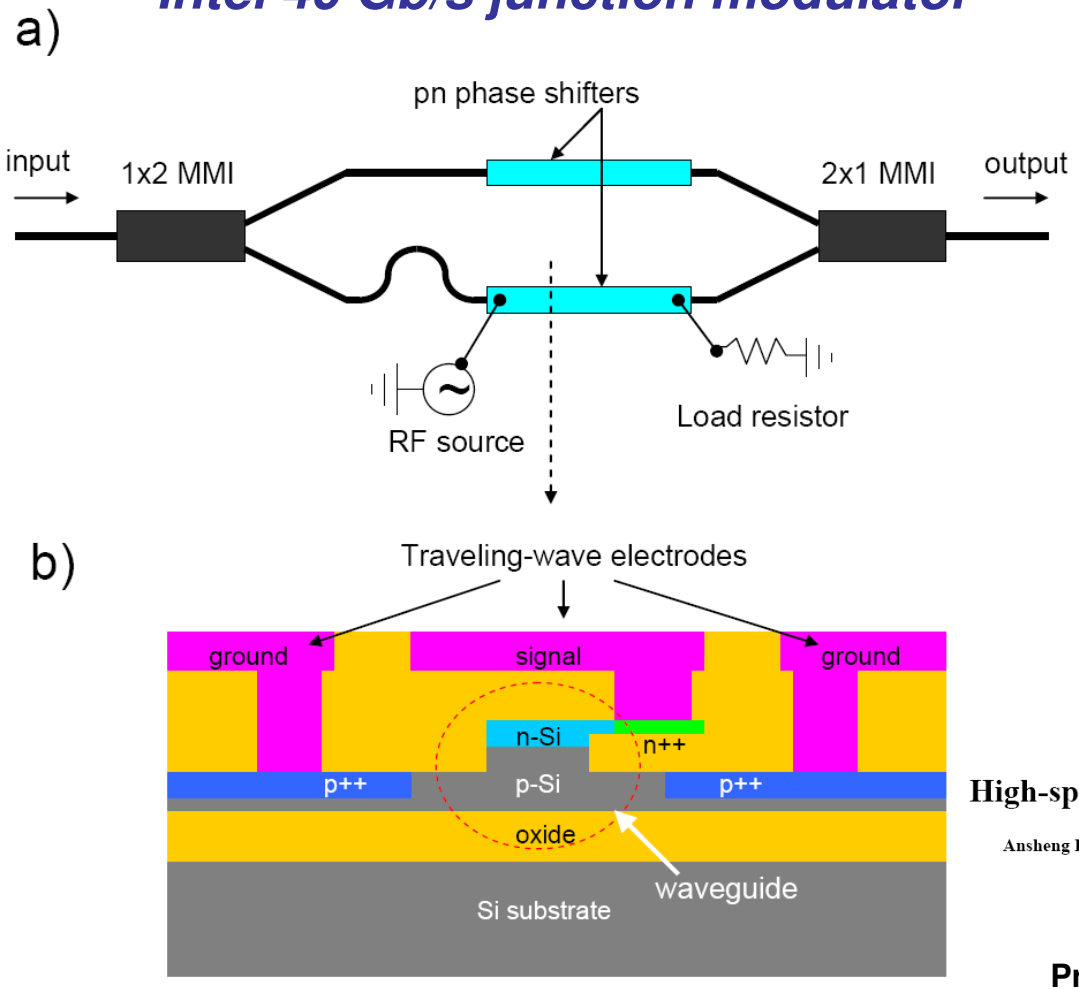
CMOS Optical Modulator with Differential Driver

Details presented at ISSCC 2006, A Huang, et al.

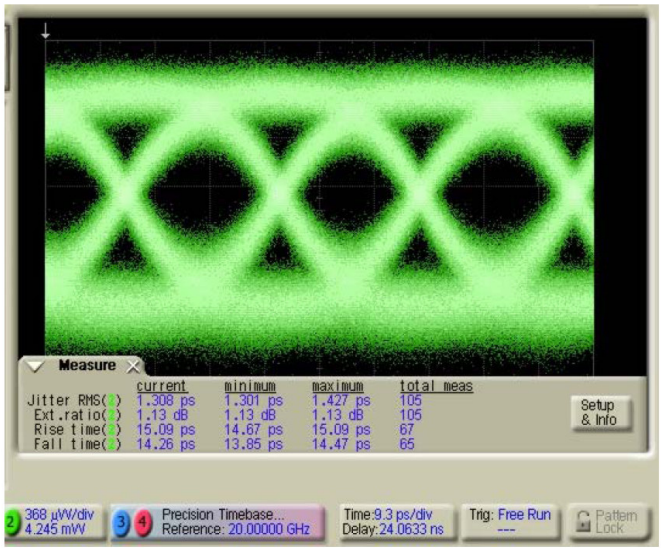


Modulators

Intel 40 Gb/s junction modulator



(a) Plan view of modulator architecture, and (b) lateral cross section of horizontal junction, vertical depletion ridge waveguide active section



40 Gb/s eye diagram

IMD3.pdf

High-speed Silicon Modulator for Future VLSI Interconnect

Ansheng Liu[1], Ling Liao[1], Doron Rubin[2], Juthika Basak[1], Hat Nguyen[1], Yoel Chetrit[2], Rami Cohen[2], Nahum Izhaky[2], and Mario Paniccia[1]

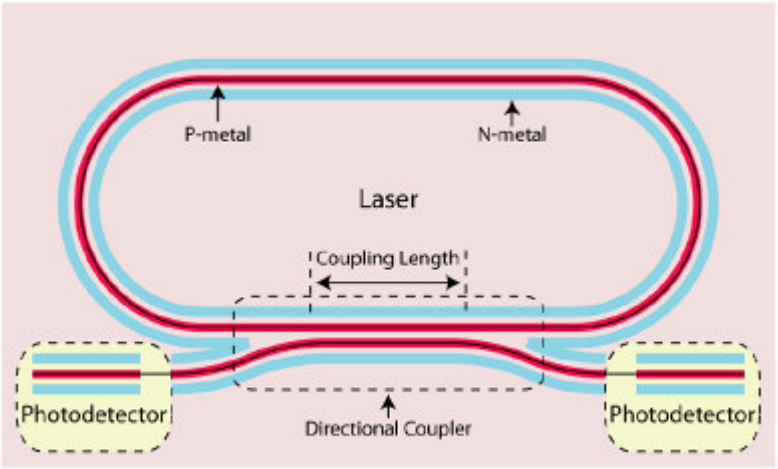
[1]*Intel Corporation, 2200 Mission College Blvd, SC12-326, Santa Clara, CA 95054*

[2]*Intel Corporation, S.B.I Park Har Hotzvim, Jerusalem, 91031, Israel*

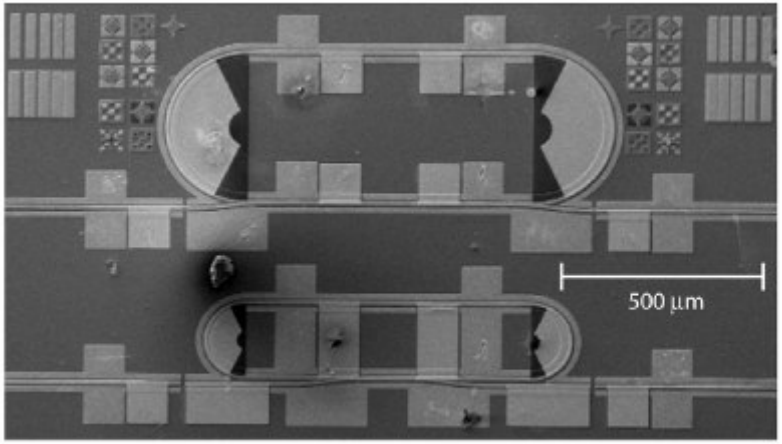
Ansheng.liu@intel.com

Presented at IPNRA, Salt Lake City, July 2007

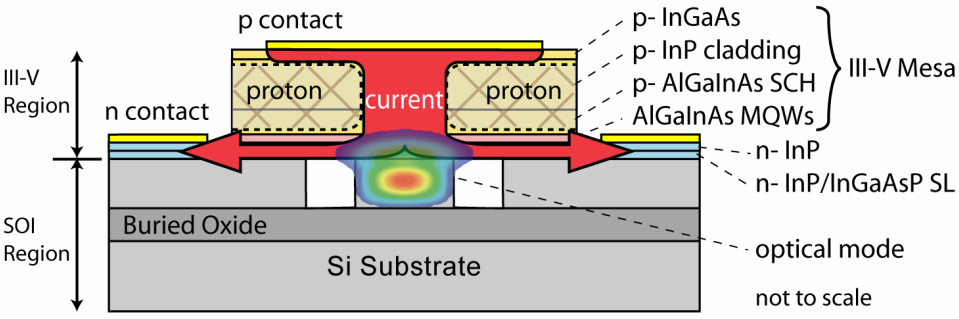
Hybrid Materials & Wafer Bonding Techniques - UCSB & Intel

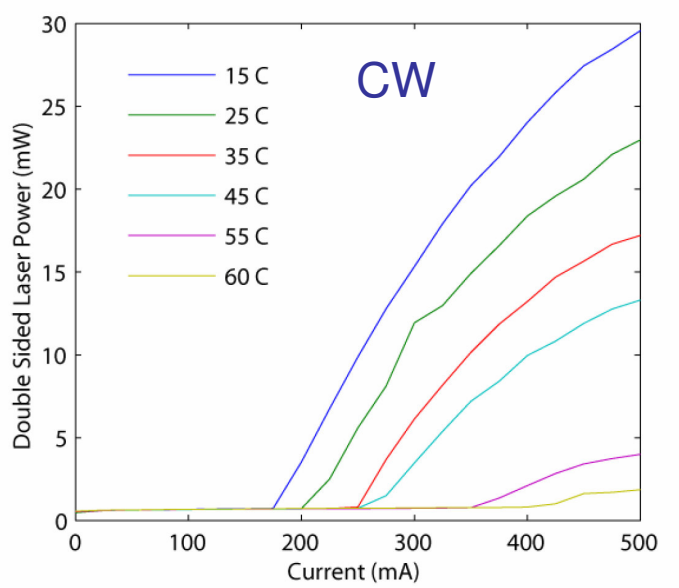


(a)



(b)





Integrated AlGaInAs-silicon evanescent racetrack laser and photodetector

Alexander W. Fang[1], Richard Jones[2], Hyundai Park[1], Oded Cohen[3], Omri Raday[3], Mario J. Paniccia[2], & John E. Bowers[1]

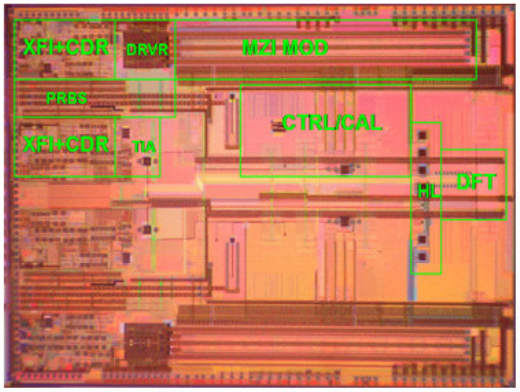
5 March 2007 / Vol. 15, No. 5 / OPTICS EXPRESS 2316

University of California Santa Barbara

3 CMOS Photonics Chips:

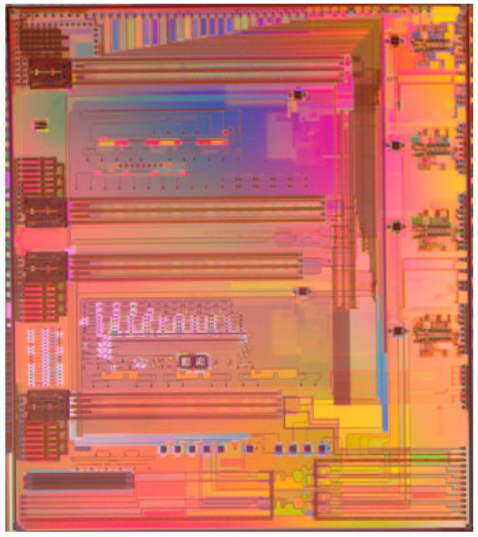
SAMPLING NOW!

Aurora



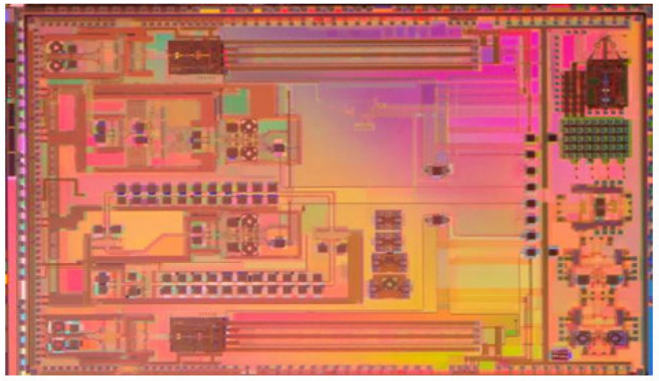
Two independent 10Gb transceivers on a single die (contains complete PHY circuitry)

Pulsar



A single 40Gb WDM transceiver
4λ x 10Gb
(PMD circuits only)

Beacon



Two ultra-low phase noise 10GHz RF oscillators

Where is this work on photonic integration being done?

Current North American Centers of Photonic Integration:

- **Industry**
  - **Products on market or product introduction plans**
    - JDSU
    - Infinera
    - CyOptics
    - Luxtera
    - Kotura
    - SiOptical
    - OneChip Photonics
    - ???
  - **R&D Centers**
    - Alcatel-Lucent (Bell Labs)
    - MIT Lincoln Labs
    - IBM
    - Intel
    - ???
- **University:**
  - **Full operational PIC fab & test infrastructure**
    - UCSB
    - UC Davis
    - ???
  - **PIC technology development & evaluation**
    - Caltech
    - USC
    - MIT
    - UIUC
    - Stanford
    - Berkeley
    - UCLA
    - UCSD
    - Univ. of Maryland
    - Univ. of Michigan
    - Univ. of Wisconsin
    - Lehigh
    - BU
    - Univ. of Delaware
    - Univ. of Washington
    - Univ. of Central Florida
    - …

Photonic integrated technology development

Photonic Integration challenges/opportunities:

- *Continue to shrink active photonic components, scale PIC densities*
  - *Identify fundamental limits & validate*
- *Mature modeling & CAD tools for PICs*
- *Take advantage of potential for embedded intelligence in PICs*
- *Still need new packaging concepts at PIC and line card level*
  - *Final answer can't be high-density line cards with massive fiber spaghetti*

Big Questions for Integration

What do you think are the three most important ways that photonic integration could impact future internet capabilities and services?

Examples:

- cost, size, power reduction of current subsystem architectures & obvious roadmap extensions
- integrate to achieve dramatically higher raw performance or reliability than can be realized with today's subsystems technology
- provide the enabling cost reduction to extend ultra-high bandwidth to the network edge
- dramatic cost-reduction to enable the ubiquitous realization of today's all-optical networking architecture concepts
- produce practical all-optical wavelength conversion
- enable practical ultra-high-speed optical packet switching
- dramatic cost-reduction in OE conversion to obviate analog optical networking concepts and facilitate all-digital data management
- unprecedented new levels of agility in optical layer bandwidth management
- enable dramatic new board-to-board or chip-to-chip interconnection (i.e., *in the box*)
- migrate all the way into *on-chip* data distribution for higher performance processors for computing/switching
- realizing unforeseen or otherwise impractical new functionality to enable entirely new network architectures

Some Drivers for Integration

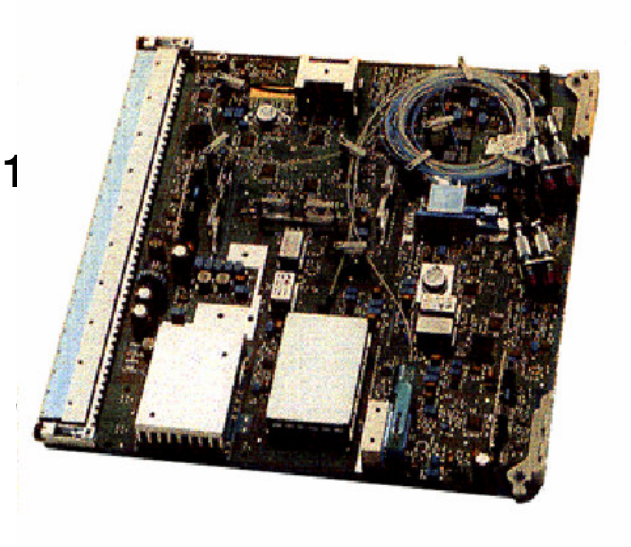
General: Reductions in cost, size, power

Some specific drivers:

- ***Line card density***
  - **Allow optical solutions to achieve electrical solution densities but at orders of magnitude higher rate**
- ***OEO cost reduction in WDM transport***
  - **Enable economics for full digital management at all network nodes**
- ***Practical realization of optical networking functionality***
  - **All-optical regeneration**
  - **High-performance λ conversion**
  - **Optical packet switching architectures**

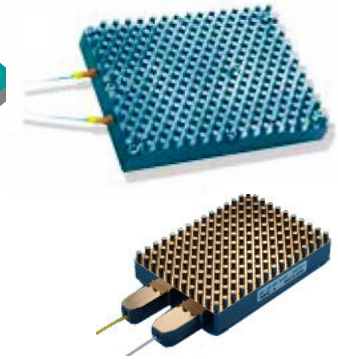
Transceiver Trends

Old line card solution



1997
Discrete board assembly
25W

300 pin MSA
127mm x 127mm x 18mm
DWDM 8W typ 14W max
SFF 300 pin MSA
77mm x 55mm x 16mm
DWDM – 5 - 8W Typ



2001
Transponder:
Subsystem in a package

Xenpak

XFP

SFP+

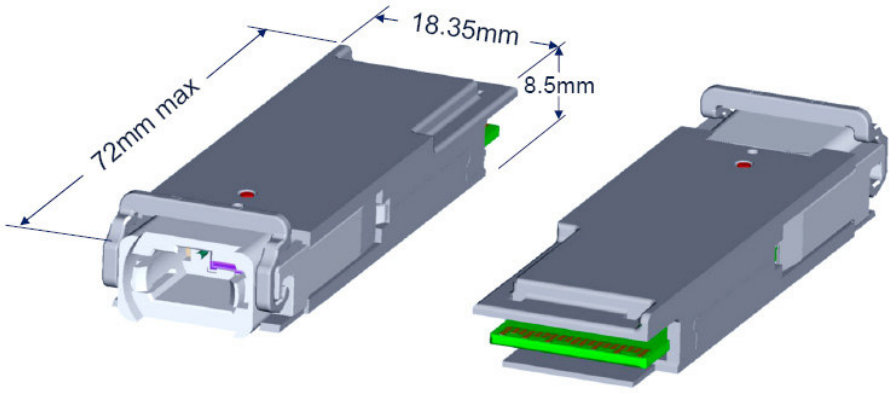
Form factor comparison			
Form factor	Size (inches)	Maximum DC power dissipation (W)	Maximum slots per line card
XENPAK	4.7×2	6	8
X2	2.7×1.6	4	16
XFP	2.7×0.7	2.5	30
SFP+	2×0.5	1	48

SFP+ transceivers emerge as key 10GbE trend
by Scott Schube
Lightwave December, 2006

Transceiver Trends

General: Reductions in cost, size, power

- Line card density:
  - From one Tx/Rx per line card to up to ***48*** SFP+ transceivers per card!
  - Power: From > 25W to < 0.6W at 10 Gb/s
- Transceiver functionality
  - After initial thrust to build in more PHY electronics, returning to simple optics
  - Integrate more electrical functionality on shared VLSI Si on line card board
- Next in line: QSFP MSA?
  - 4 x 10Gb/s
  - < 3.5W power
  - Targeting practical standard 40G



Front View Back View

Big Questions for Integration

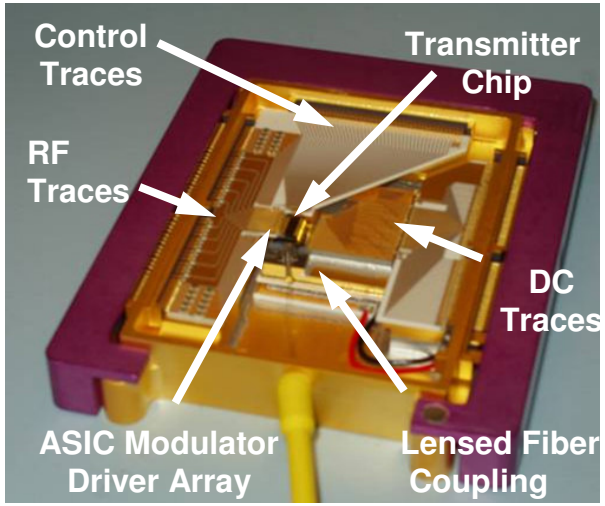
What is the role of photonic integration in enabling reductions in transceiver cost, size and power?

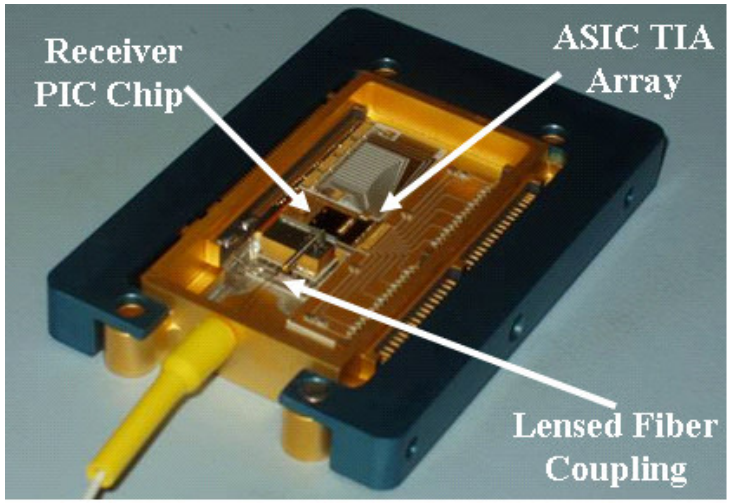
Big Questions for Integration

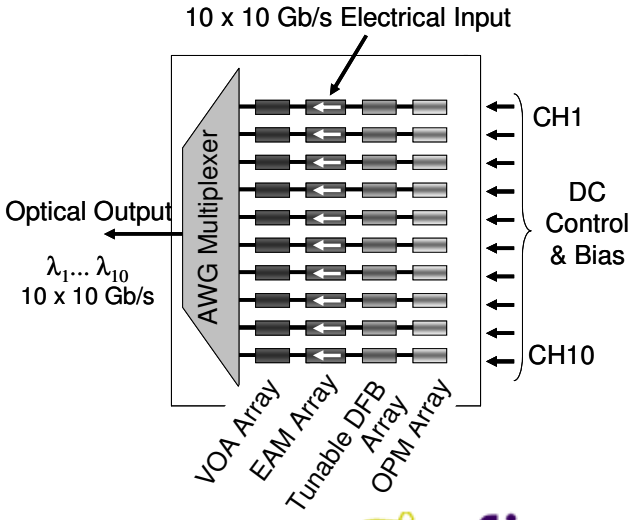
What is the role of photonic integration in enabling required reductions in cost, size and power?

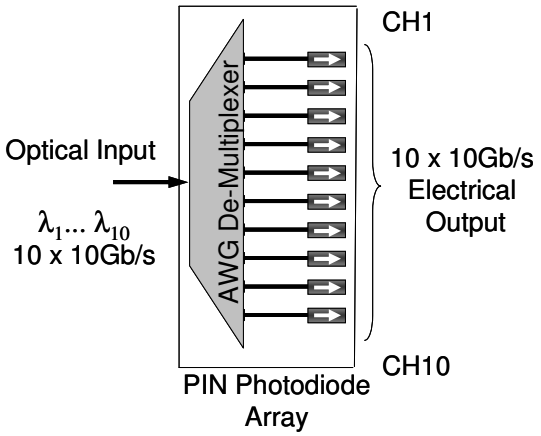
- Today's annual depreciated line card cost is being overtaken by the annual cost of the power to operate it! *(Ashok Krishnamoorthy, Sun)*
  - Power not just a density limiter from thermal dissipation, it is on track to become the *only thing that matters!*
    - Optical active device size scaling and integration are *critical* enablers to continued power (& size, cost) reduction
    - Optical loss is key contributor to power consumption, losses can be reduced by integration
  - *Advances in integration will be essential for next-generation internet to reach its potential*

100 Gb/s LS-PIC DWDM Transmit & Receive Modules





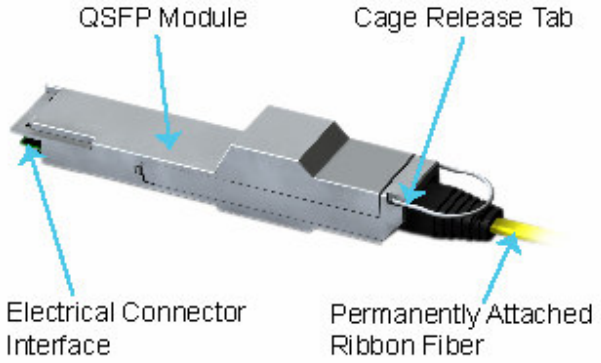




infinera

CLEO 2005, 100Gb/s DWDM PICs, FK, Infinera, 1322 Bordeaux Dr., Sunnyvale, CA 94089

Blazar LUX5010 Multirate 4x10G Optical Active Cable



Features	Benefits
Optical Active Cable: Closed Optical System	▪ No optical interoperability issues ▪ Easy maintenance - no need to clean optics ▪ Eliminates costly fiber connectors
Multi-Rate (1-10Gbps)	▪ One solution for multiple applications
Single Laser for 4-Channels	▪ Better reliability
SFP+ Electrical Interface	▪ Standards compliant electrical interface (IB, FC, 10GbE) ▪ Lower link costs: 8 CDRs eliminated (4 per end)
Single-Mode Optics	▪ Lower link costs and better performance ▪ Supports reach up to 300 meters for QDR (4x10Gbps) ▪ Eliminates need for EDC Components
Hot-Pluggable	▪ Field replaceable
QSFP Form-factor	▪ Provides more bandwidth density
Low Power (0.5W/10G)	▪ Lower cooling costs and simplified thermal management

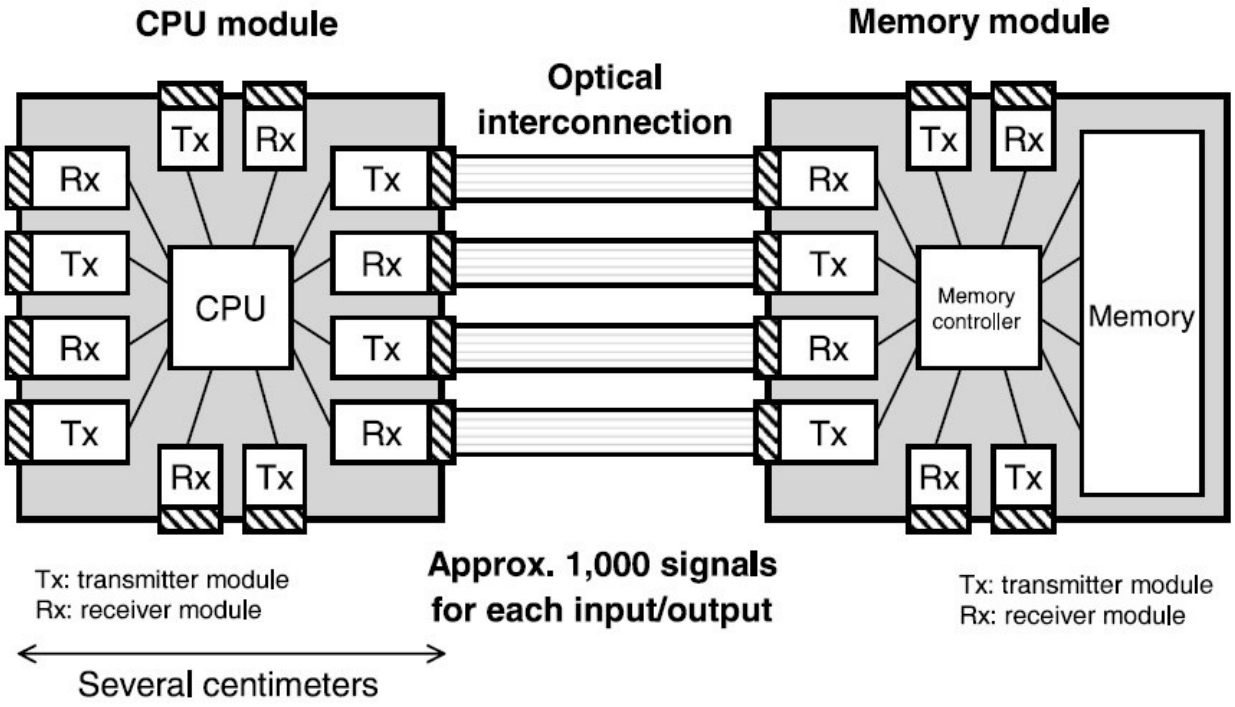
Big Questions for Integration

What is the role of photonic integration in enabling these reductions in cost, size and power?

- Apart from limited (but important) examples of key performance benefits from serial integration, most photonic integration applications seem to pay off with increased ***parallelism***
  - WDM functionality is inherently highly parallel
  - Even QSFP transceiver is 4-wide, for Luxtera example power, cost savings comes from 4 transceivers fed by one laser. Significantly less savings with just one channel.
- Looking at line card trends, can integration extend to 16 or more ports from a single chip? (probably yes)
- Looking at WDM, can integration extend to 40 λ's or more on a single chip? (research demos suggests yes)
- Can integration with improved actives provide fundamental power reduction? (physics suggests yes)

Photonic integrated technology development

Probable key role in enabling computer, router, and switch platforms to continue to scale in bandwidth & processing power:



Kanji Takeuchi, Science and Technology Trends, Quarterly Review No. 20, July 2006

Photonic integrated technology development

Some additional outstanding PIC opportunities & areas for impact:

- *Computational platforms employing optical networking concepts?*
  - *(i.e., not just as low-latency, low-power links)*
  - *At board level*
  - *At chip level*
- *Can PICs help achieve ultimate limits of spectral density?*
  - *Electrical optical intimacy*
  - *Complex but stable, compact, low-power, low-cost optical subassemblies*
  - *Example: Opportunity for renewed focus on **coherent optical communications?***
    - *Use CMOS for filtering rather than physical optical inteferometric designs*
    - *Ready implementation of sophisticated high-spectral density coding (think wireless technology)*
    - *Rapid bandwidth allocation*
    - *Not for core – instead, ultimate access network technology?*

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Photonic integrated technology development

How can GENI help in development of photonic integration?

- *Help to reveal and develop solutions to vexing underlying problems with scaling the future internet*
  - *Provide insights in vertically integrated teams to promote appropriate PIC focus directions*
- *Provide venue for evaluating new PIC functionality in context of evolving GENI testbeds*