# NetFPGA Update at GEC4

http://NetFPGA.org/

**NSF GENI Engineering Conference 4 (GEC4)**
**March 31, 2009**


## John W. Lockwood

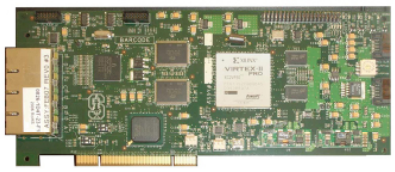
**http://stanford.edu/~jwlockwd/**
**jwlockwd@stanford.edu**


Hardware and tools available for university programs thanks to grants, donations, and/or partnerships from:



# What is the NetFPGA?

**A line-rate, flexible, open networking platform for teaching and network research**



=

- Network Interface Card
- Hardware Accelerated Linux Router
- IPv4 Reference Router
- Traffic Generator
- Openflow Switch
- List of All Projects
- Add Your Project

# Goals for GENI Network Substrate

- **Easily compose Systems**
  - By combining multiple, standard elements
- **Clearly define the functionality**
  - Functionality defined through regression tests
- **Widely disseminate projects**
  - Open-source code downloads and installs with yum
  - Projects documented on Web, Wiki, Blog, & Facebook
- **Build a community of developers**
  - Organize projects
  - Document contributions
  - Respond to feedback from users
  - Encourage the community to contribute



# Strengths of Reconfigurable Networks

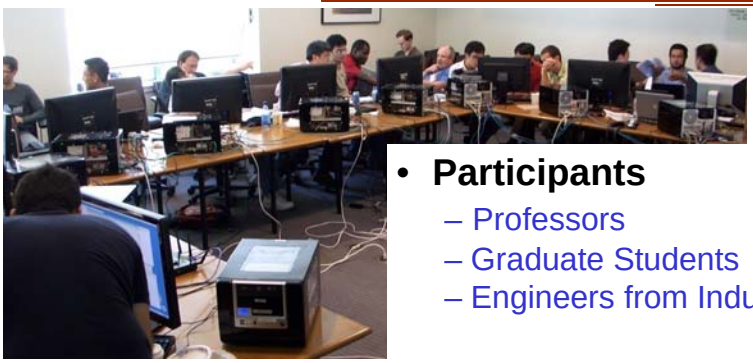
- **Implement Wire-speed Processing**
  - Header Processing
    - Switching, routing, firewalls
  - Full Payload Processing
    - Content distribution and intrusion prevention
- **Enhance and create new datapath functions**
  - Monitor network flows
    - NetFlow probe
  - Control network flows
    - OpenFlow switch
  - Generate traffic
    - Traffic generator
  - Process new protocols ..
    - Reference Router
- **Power efficient**
  - Datapath optimized for switching

# Why do we use the NetFPGA

- **To run laboratory courses on network routing**
  - Professors teach courses (CS344, Workshops, ..)
- **To teach students how to build real Internet routers**
  - Train students to build routers (Cisco, Juniper, Huawei, .. )
- **To research how new features in the network**
  - Build network services for data centers (Google, UCSD.. )
- **To prototype systems with live traffic**
  - That Buffer measurement (while maintaining throughput, ..)
- **To help hardware vendors understand device requirements**
  - Use of hardware (Xilinx, Micron, Cypress, Broadcom, ..)



# NetFPGA Summer Camp



- **Participants**
  - Professors
  - Graduate Students
  - Engineers from Industry

- **Format : One week event**
  - 2.5 Days of Training on the reference router
  - 2 Days to work on projects
  - Final Projects presented on Friday Afternoon

# Photos from NetFPGA Tutorials

SIGCOMM - Seattle, Washington, USA

Beijing, China

SIGMETRICS - San Diego, California, USA

EuroSys - Glasgow, Scotland, U.K.

Bangalore, India

http://netfpga.org/pastevents.php and http://netfpga.org/upcomingevents.php



# Where are NetFPGAs?

- Over 500 users with ~1,000 cards deployed
- Deployed in ~120 universities in 17 Countries

# NetFPGA Hardware in North America

**Locations of Deployed NetFPGA Hardware** — **USA - Jan 2009**




# NetFPGA Hardware in Europe

**Locations of Deployed NetFPGA Hardware** — **EU - Jan 2009**

# NetFPGA Hardware in Asia

**Locations of Deployed NetFPGA Hardware**




# NetFPGA Systems

- **Pre-built systems available**
  - From 3rd Party Vendor
- **PCs assembled from parts**
  - Integrates into standard PC
- **Details are in the Guide**
  - http://netfpga.org/static/guide.html

# Rackmount NetFPGA Servers

2U Server
(Dell 2950)

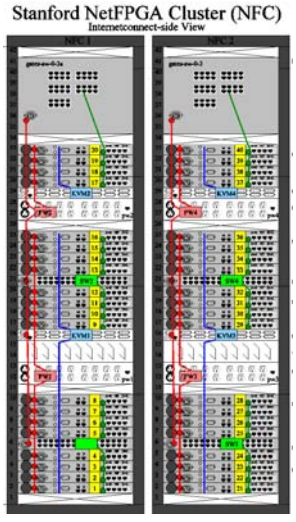
NetFPGA inserts in
PCI or PCI-X slot

1U Server
(Accent Technology, Inc)

Thanks: Brian Cashman for providing machine



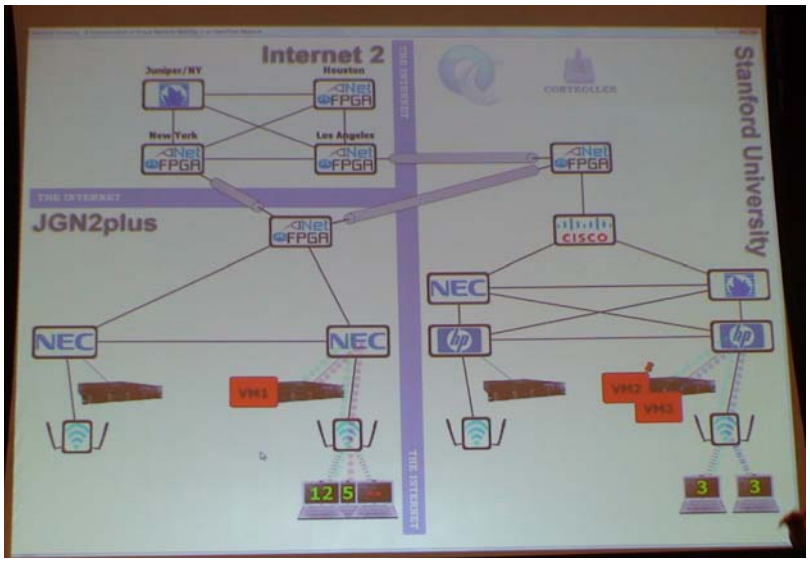
# Stanford NetFPGA Cluster




Statistics

- Rack of 40
  - 1U PCs
  - NetFPGAs
- Manged
  - Power,
  - Console
  - VLANs
- Provides 160 Gbps of full line-rate processing bandwidth

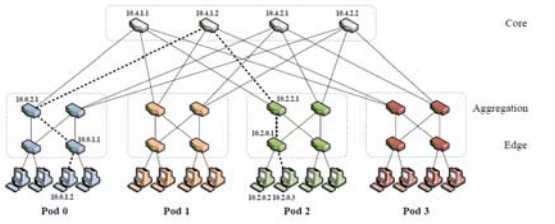
# NetFPGAs in the Internet 2 & Japan

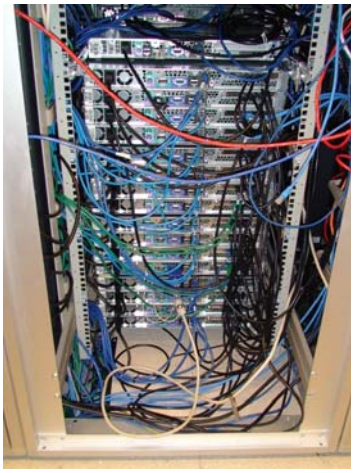



From GENI Engineering Conference – Oct 2008



# UCSD-NetFPGA Cluster



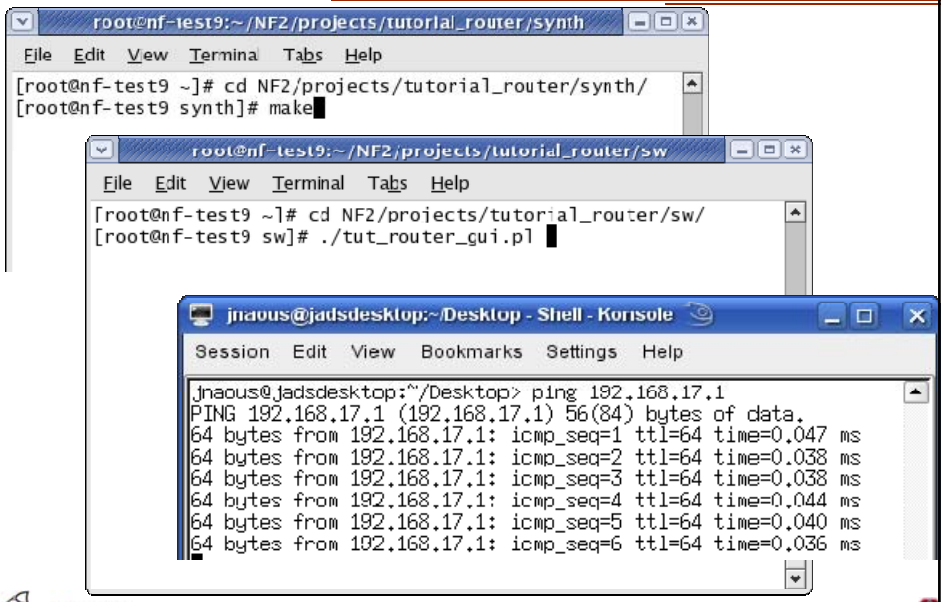



# Building the NetFPGA route from the Verilog Source Code

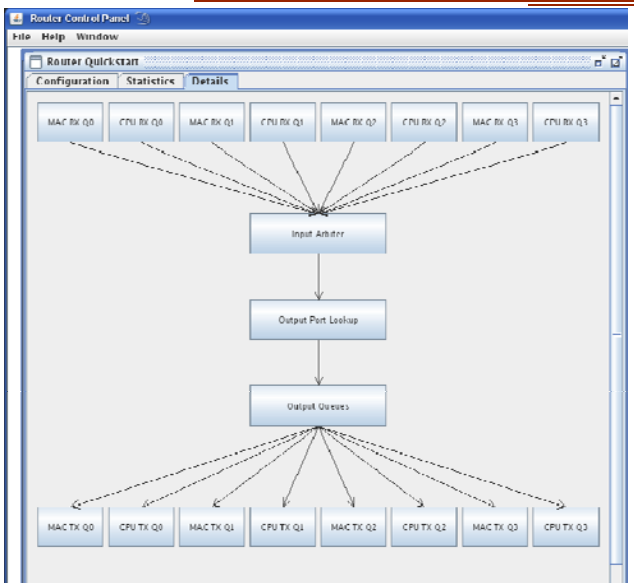
## Using the Xilinx ISE tools to synthesize the logic for the FPGA



# Building the NetFPGA Router



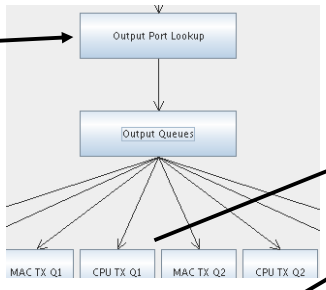
# Explore the Router

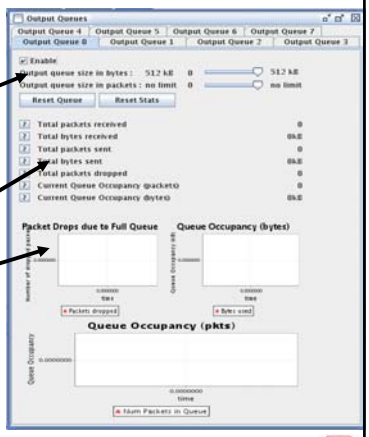





# Look inside the Router

Click



## Preview of Upcoming 2.0 Release

- **Modular Registers**
  - Simplifies integration of multiple modules
    - Many users control NetFPGAs from software
  - Register set joined together at build time
    - Project specifies registers in XML list
- **Packet Buffering in DRAM**
  - Supports Deep buffering
    - Single 64MByte queue in DDR2 memory
- **Programmable Packet Encapsulation**
  - Packet-in-packet encapsulation
    - Enables tunnels between OpenFlowSwitch nodes



## Conclusions

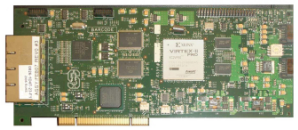
- **NetFPGA Provides**
  - Open-source, hardware-accelerated Packet Processing
  - Modular interfaces arranged in reference pipeline
  - Extensible platform for packet processing
- **NetFPGA Reference Code Provides**
  - Large library of core packet processing functions
  - Scripts and GUIs for simulation and system operation
  - Set of Projects for download from repository
- **The NetFPGA Community of Developers use**
  - Well defined functionality defined by regression tests
  - Blogs that organize projects
  - Wiki pages that Document contributions
  - Forum for discussion of feedback from users

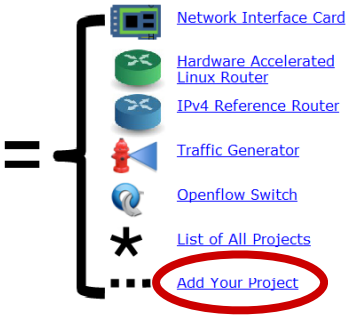
# NetFPGA Developers Workshop

## August 13-14, 2009 at Stanford University

- **You already know that the NetFPGA implements a Gigabit NIC, a hardware-accelerated Internet router, a traffic generator, an OpenFlow switch, a NetFlow probe and more. What else can it do? We invite you, our worldwide NetFPGA Developers, to show off your project. Submit a paper to describe your project, prepare a demo, and come to Stanford in August to demonstrate your work!**

- **Papers Due:**
  - April 20, 2009
- **Workshop Date:**
  - Aug. 13-14, 2009
- **Paper Format:**
  - 4-8 page, ACM-style
- **Demonstrations:**
  - Run on NetFPGA(s)
- **Program Chairs:**
  - John W. Lockwood (Stanford University)
  - Andrew W. Moore (Cambridge University)
- **Full Details**
  - http://NetFPGA.org/DevWorkshop






**"What have you built with your NetFPGA?"**



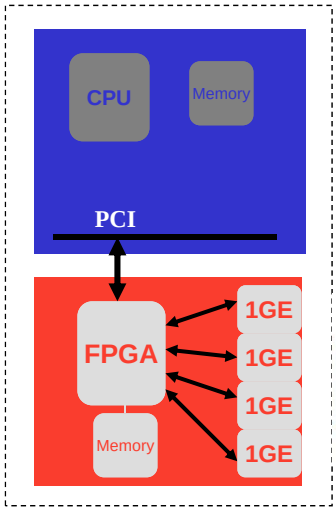
# Additional Slides

# What is a NetFPGA System

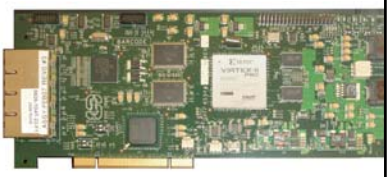
**Software running on a standard PC**

**+**

**A hardware accelerator built with Field Programmable Gate Array driving Gigabit network links**




PC with NetFPGA

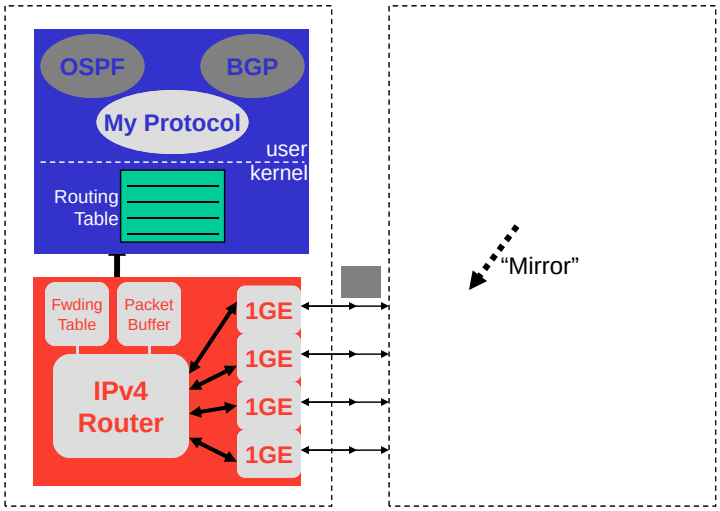


NetFPGA Board



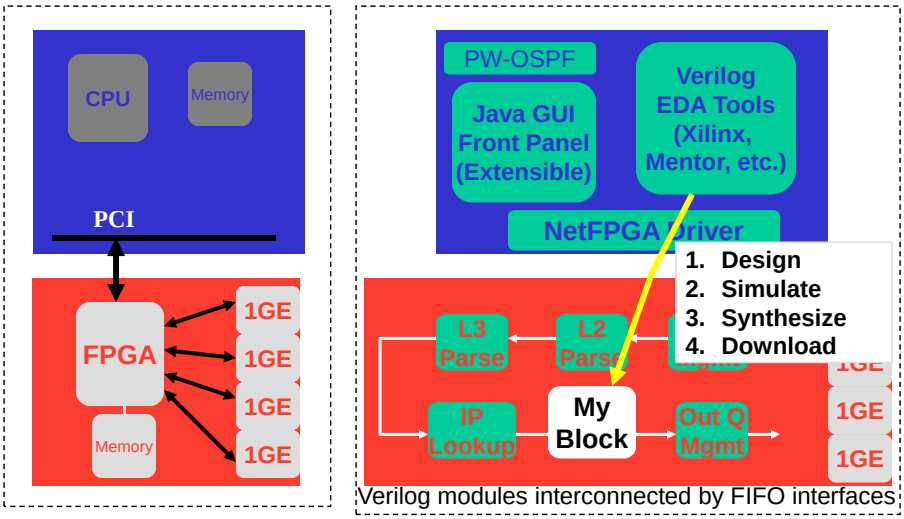
# How do I Run the Router Kit

**User-space development, 4x1GE line-rate forwarding**



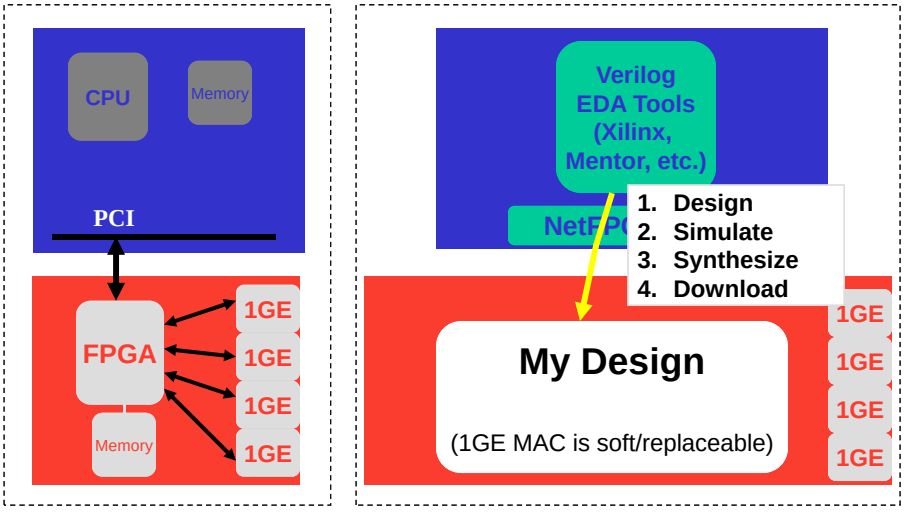
Usage #2

# Building Modular Router Modules

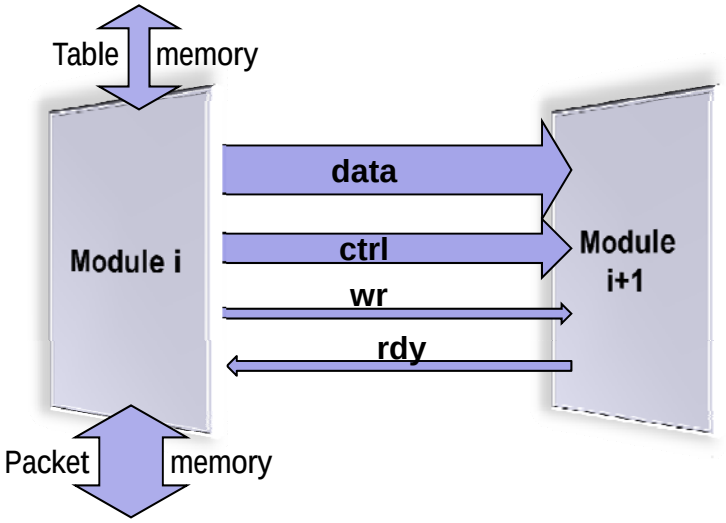





# How do I create new systems

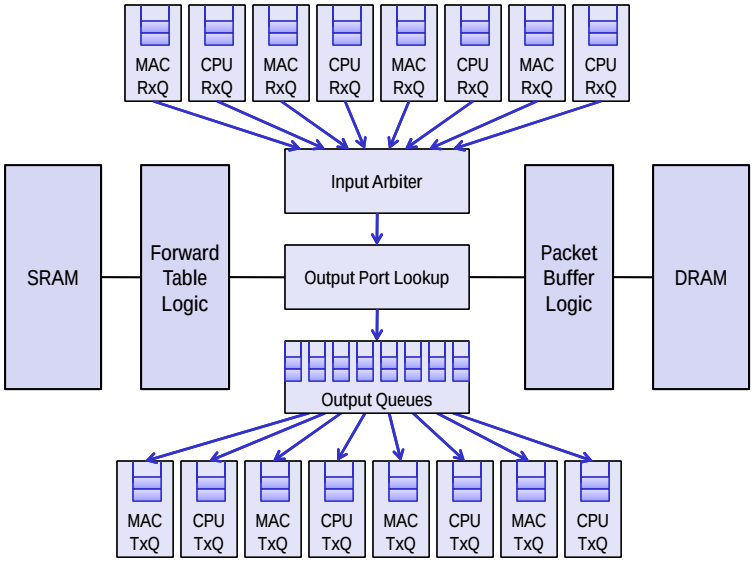


# Inter-module Communication






# NetFPGA 1G Pipeline Stages



# Need Help? – See Discussion Forums




# Acknowledgements

**Support for the NetFPGA project is provided by the following organizations, companies, and institutions**

Disclaimer: Any opinions, findings, conclusions, or recommendations expressed in this material do not necessarily reflect the views of the National Science Foundation or of any other sponsors supporting this project.

# Learn more About the NetFPGA

http://NetFPGA.org/

-or-

Google: "NetFPGA"

**Learn More**

Project summary, videos, publications, tutorials

**Get Started**

Obtain NetFPGA hardware, download gateware & software, review reference designs

**Develop**

Create user account, contribute your code, document your project