

NetFPGA Update at GEC4



<http://NetFPGA.org/>

NSF GENI Engineering Conference 4 (GEC4)
March 31, 2009

John W. Lockwood

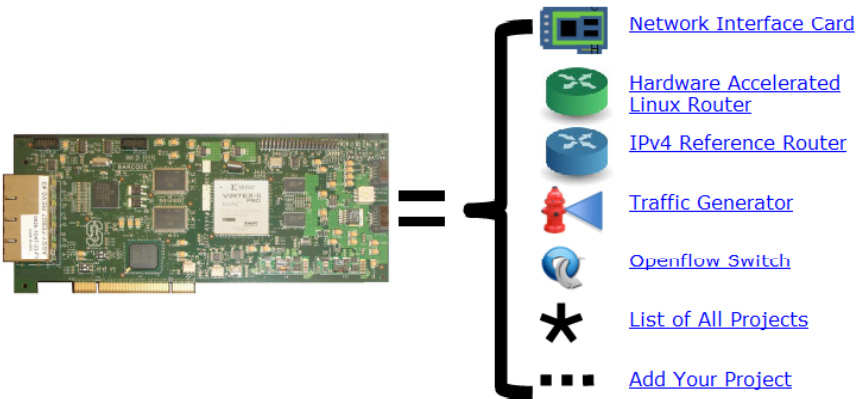
<http://stanford.edu/~jwlockwd/>
jwlockwd@stanford.edu

Hardware and tools available for university programs thanks to grants, donations, and/or partnerships from:



What is the NetFPGA?

A line-rate, flexible, open networking platform for teaching and network research



Goals for GENI Network Substrate

- **Easily compose Systems**
 - By combining multiple, standard elements
- **Clearly define the functionality**
 - Functionality defined through regression tests
- **Widely disseminate projects**
 - Open-source code downloads and installs with yum
 - Projects documented on Web, Wiki, Blog, & Facebook
- **Build a community of developers**
 - Organize projects
 - Document contributions
 - Respond to feedback from users
 - Encourage the community to contribute

Strengths of Reconfigurable Networks

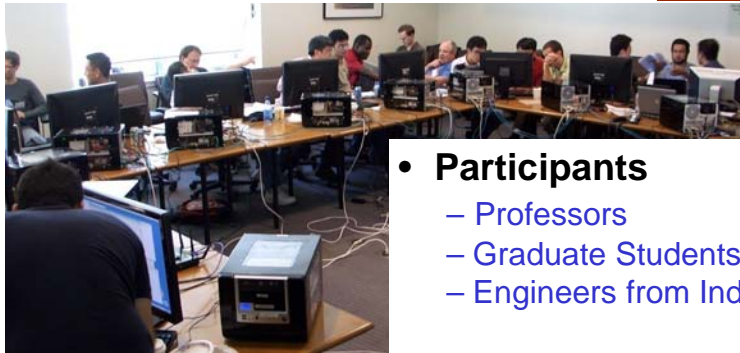
- **Implement Wire-speed Processing**
 - Header Processing
 - Switching, routing, firewalls
 - Full Payload Processing
 - Content distribution and intrusion prevention
- **Enhance and create new datapath functions**
 - Monitor network flows
 - NetFlow probe
 - Control network flows
 - OpenFlow switch
 - Generate traffic
 - Traffic generator
 - Process new protocols ..
 - Reference Router
- **Power efficient**
 - Datapath optimized for switching

Why do we use the NetFPGA

- **To run laboratory courses on network routing**
 - Professors teach courses (CS344, Workshops, ..)
- **To teach students how to build real Internet routers**
 - Train students to build routers (Cisco, Juniper, Huawei, ..)
- **To research how new features in the network**
 - Build network services for data centers (Google, UCSD..)
- **To prototype systems with live traffic**
 - That Buffer measurement (while maintaining throughput, ..)
- **To help hardware vendors understand device requirements**
 - Use of hardware (Xilinx, Micron, Cypress, Broadcom, ..)



NetFPGA Summer Camp



- **Participants**
 - Professors
 - Graduate Students
 - Engineers from Industry

- **Format : One week event**
 - 2.5 Days of Training on the reference router
 - 2 Days to work on projects
 - Final Projects presented on Friday Afternoon



Photos from NetFPGA Tutorials



SIGCOMM - Seattle, Washington, USA



Beijing, China



SIGMETRICS - San Diego, California, USA



Bangalore, India



EuroSys - Glasgow, Scotland, U.K.

<http://netfpga.org/pastevents.php> and <http://netfpga.org/upcomingevents.php>

Where are NetFPGAs?

- Over 500 users with ~1,000 cards deployed
- Deployed in ~120 universities in 17 Countries



NetFPGA Hardware in North America

Locations of Deployed NetFPGA Hardware

USA - Jan 2009



NetFPGA Hardware in Europe

Locations of Deployed NetFPGA Hardware

EU - Jan 2009



NetFPGA Hardware in Asia

Locations of Deployed NetFPGA Hardware



NetFPGA Systems

- **Pre-built systems available**
 - From 3rd Party Vendor
- **PCs assembled from parts**
 - Integrates into standard PC
- **Details are in the Guide**
 - <http://netfpga.org/static/guide.html>



Rackmount NetFPGA Servers



2U Server
(Dell 2950)



NetFPGA inserts in
PCI or PCI-X slot

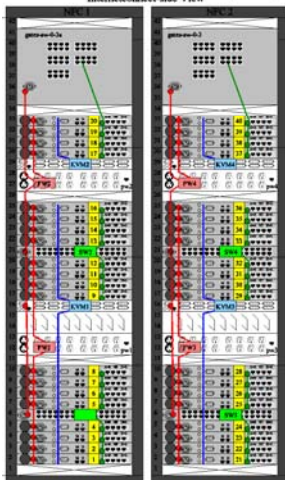


1U Server
(Accent Technology, Inc)

Thanks: Brian Cashman for providing machine

Stanford NetFPGA Cluster

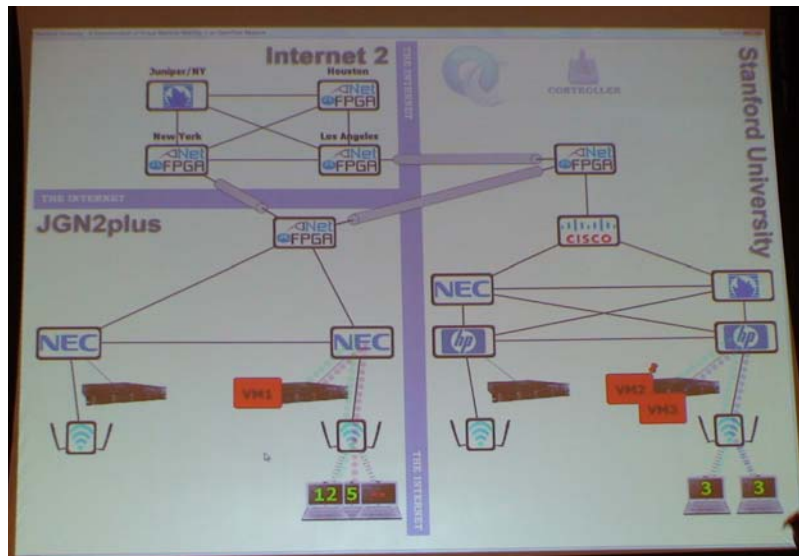
Stanford NetFPGA Cluster (NFC)
Internetconnect-side View



Statistics

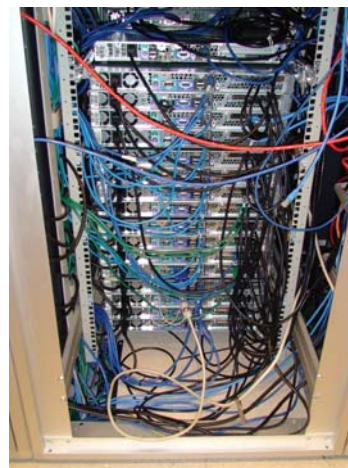
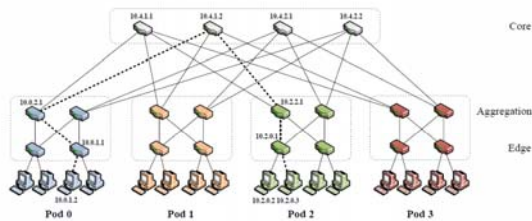
- Rack of 40
 - 1U PCs
 - NetFPGAs
- Manged
 - Power,
 - Console
 - VLANs
- Provides 160 Gbps of full line-rate processing bandwidth

NetFPGAs in the Internet 2 & Japan



From GENI Engineering Conference – Oct 2008

UCSD-NetFPGA Cluster



Building the NetFPGA route from the Verilog Source Code

Using the Xilinx ISE tools to
synthesize the logic for the FPGA

Building the NetFPGA Router

The screenshot shows three overlapping terminal windows. The top window is titled 'root@nf-test9:~/NF2/projects/tutorial_router/synth' and shows the command 'make' being executed. The middle window is titled 'root@nf-test9:~/NF2/projects/tutorial_router/sw' and shows the command './tut_router_gui.pl' being executed. The bottom window is titled 'jnaous@jadsdesktop:~/Desktop - Shell - Konsole' and shows the output of a 'ping' command to 192.168.17.1, with six successful responses and their respective times.

```
root@nf-test9:~/NF2/projects/tutorial_router/synth
File Edit View Terminal Tabs Help
[root@nf-test9 ~]# cd NF2/projects/tutorial_router/synth/
[root@nf-test9 synth]# make

root@nf-test9:~/NF2/projects/tutorial_router/sw
File Edit View Terminal Tabs Help
[root@nf-test9 ~]# cd NF2/projects/tutorial_router/sw/
[root@nf-test9 sw]# ./tut_router_gui.pl

jnaous@jadsdesktop:~/Desktop - Shell - Konsole
Session Edit View Bookmarks Settings Help
jnaous@jadsdesktop:~/Desktop> ping 192.168.17.1
PING 192.168.17.1 (192.168.17.1) 56(84) bytes of data:
64 bytes from 192.168.17.1: icmp_seq=1 ttl=64 time=0.047 ms
64 bytes from 192.168.17.1: icmp_seq=2 ttl=64 time=0.038 ms
64 bytes from 192.168.17.1: icmp_seq=3 ttl=64 time=0.038 ms
64 bytes from 192.168.17.1: icmp_seq=4 ttl=64 time=0.044 ms
64 bytes from 192.168.17.1: icmp_seq=5 ttl=64 time=0.040 ms
64 bytes from 192.168.17.1: icmp_seq=6 ttl=64 time=0.036 ms
```

Explore the Router

The screenshot shows the Router Control Panel interface. At the top, there are tabs for Configuration, Statistics, and Details. Below the tabs is a diagram illustrating the router's internal flow. It starts with eight input queues: MAC RX Q0, CPU RX Q0, MAC RX Q1, CPU RX Q1, MAC RX Q2, CPU RX Q2, MAC RX Q3, and CPU RX Q3. These queues feed into an Input Arbitrator, which then feeds into an Output Port Lookup block. The output of the Output Port Lookup block feeds into an Output Queues block. Finally, the Output Queues block feeds into eight output queues: MAC TX Q0, CPU TX Q0, MAC TX Q1, CPU TX Q1, MAC TX Q2, CPU TX Q2, MAC TX Q3, and CPU TX Q3.

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Look inside the Router

Click →

The diagram shows a click on the Output Port Lookup block in the router flow diagram. This action opens a detailed configuration window for Output Queues. The window shows the configuration for Output Queue 4, including options to Enable or Disable the queue, and sliders for Output queue size in bytes (512 KB) and Output queue size in packets (no limit). It also displays statistics for Total packets received, Total bytes received, Total packets sent, Total bytes sent, Total packets dropped, Current Queue Occupancy (packets), and Current Queue Occupancy (bytes). There are also graphs for Packet Drops due to Full Queue and Queue Occupancy (bytes).

NetFPGA 20 STANFORD UNIVERSITY

Preview of Upcoming 2.0 Release

- **Modular Registers**
 - Simplifies integration of multiple modules
 - Many users control NetFPGAs from software
 - Register set joined together at build time
 - Project specifies registers in XML list
- **Packet Buffering in DRAM**
 - Supports Deep buffering
 - Single 64MByte queue in DDR2 memory
- **Programmable Packet Encapsulation**
 - Packet-in-packet encapsulation
 - Enables tunnels between OpenFlowSwitch nodes



Conclusions

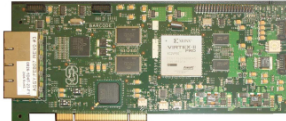
- **NetFPGA Provides**
 - Open-source, hardware-accelerated Packet Processing
 - Modular interfaces arranged in reference pipeline
 - Extensible platform for packet processing
- **NetFPGA Reference Code Provides**
 - Large library of core packet processing functions
 - Scripts and GUIs for simulation and system operation
 - Set of Projects for download from repository
- **The NetFPGA Community of Developers use**
 - Well defined functionality defined by regression tests
 - Blogs that organize projects
 - Wiki pages that Document contributions
 - Forum for discussion of feedback from users



NetFPGA Developers Workshop

August 13-14, 2009 at Stanford University

- You already know that the NetFPGA implements a Gigabit NIC, a hardware-accelerated Internet router, a traffic generator, an OpenFlow switch, a NetFlow probe and more. What else can it do? We invite you, our worldwide NetFPGA Developers, to show off your project. Submit a paper to describe your project, prepare a demo, and come to Stanford in August to demonstrate your work!
- **Papers Due:**
 - April 20, 2009
- **Workshop Date:**
 - Aug. 13-14, 2009
- **Paper Format:**
 - 4-8 page, ACM-style
- **Demonstrations:**
 - Run on NetFPGA(s)
- **Program Chairs:**
 - John W. Lockwood (Stanford University)
 - Andrew W. Moore (Cambridge University)
- **Full Details**
 - <http://NetFPGA.org/DevWorkshop>



“What have you built with your NetFPGA?”



Additional Slides

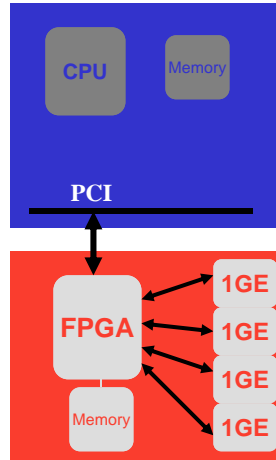


What is a NetFPGA System

Software running on a standard PC

+

A hardware accelerator built with Field Programmable Gate Array driving Gigabit network links



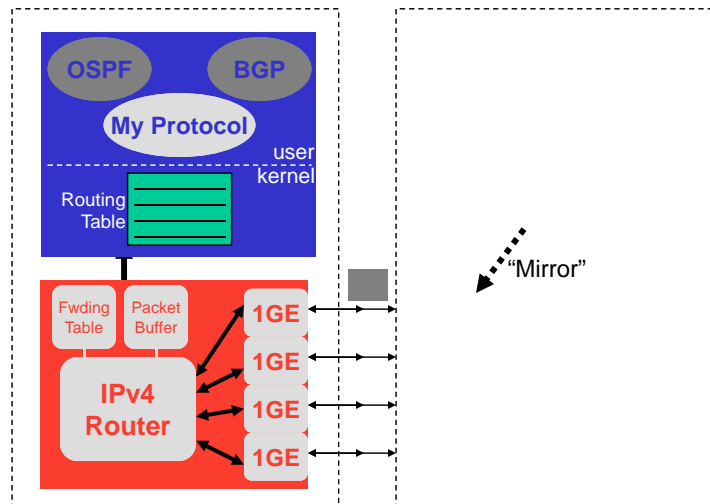
PC with NetFPGA



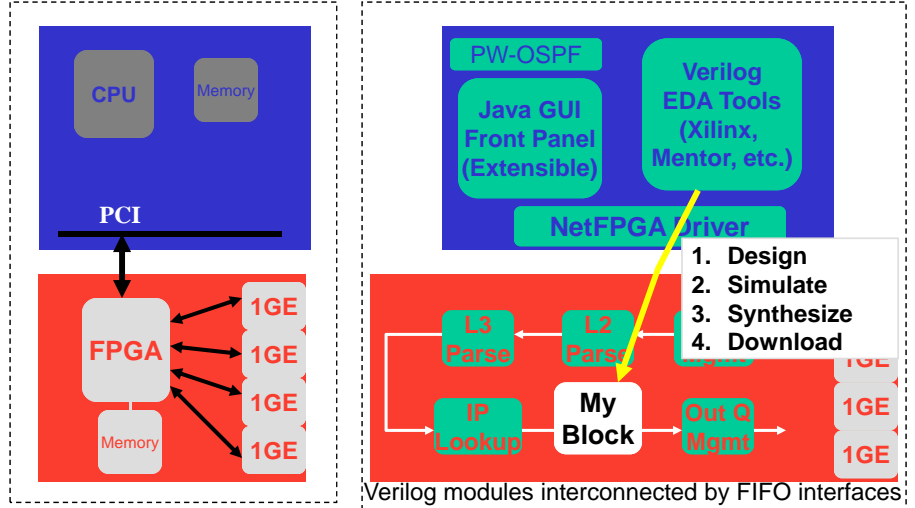
NetFPGA Board

How do I Run the Router Kit

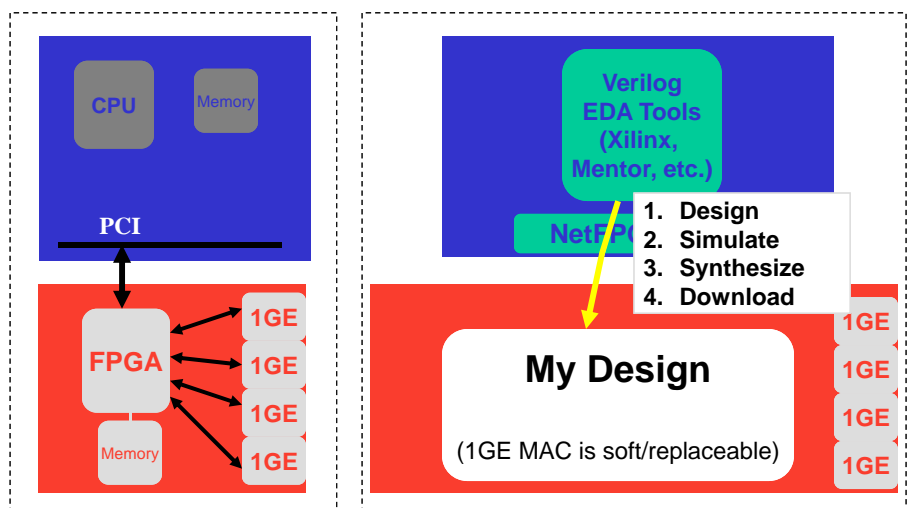
User-space development, 4x1GE line-rate forwarding



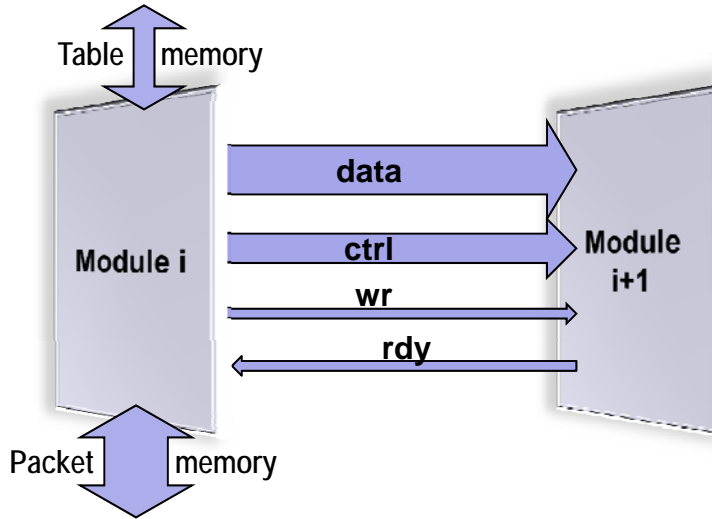
Building Modular Router Modules



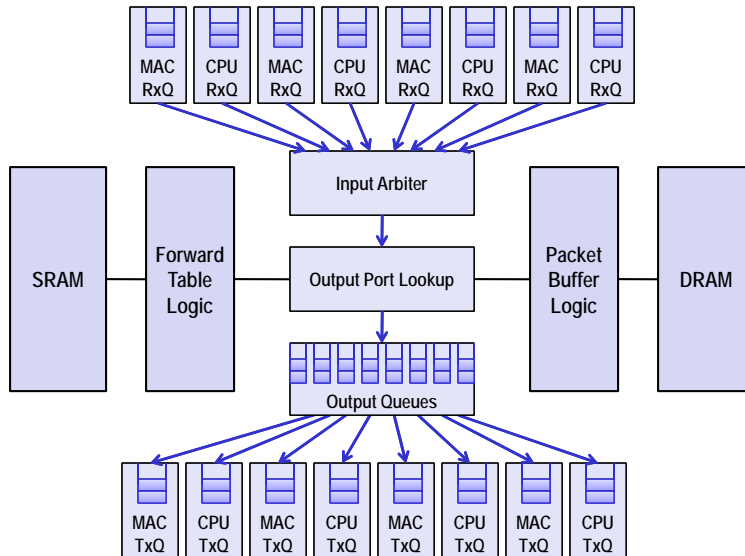
How do I create new systems



Inter-module Communication



NetFPGA 1G Pipeline Stages



Need Help? – See Discussion Forums

NetFPGA Forum

User Name Remember Me?
 Password

[Register](#)
[FAQ](#)
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[Calendar](#)
[Today's Posts](#)
[Search](#)

Welcome to the NetFPGA Forum.

If this is your first visit, be sure to check out the [FAQ](#) by clicking the link above. You may have to [register](#) before you can post: click the register link above to proceed. To start viewing messages, select the forum that you want to visit from the selection below.

Forum	Last Post	Threads	Posts
General NetFPGA discussion A forum dedicated to general NetFPGA discussion, including installation, setup and usage.			
General Discussion General discussion forum about the NetFPGA platform	 by sumeet23 02-06-2009 10:49 PM	54	209
Installation and Setup (3 Viewing) This forum should be used for discussion of installation and setup of the NetFPGA system.	 by Abhishek 02-07-2009 12:05 AM	39	179
Forum requests/queries Forum to request new forums/query existing forums.	 by gaci 01-12-2009 06:57 PM	2	3
Projects Forums dedicated to specific NetFPGA projects			
Packet Generator Discussions related to the packet generator	 by grq 01-16-2009 09:56 PM	7	34

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Acknowledgements

Support for the NetFPGA project is provided by the following organizations, companies, and institutions



Learn more About the NetFPGA

<http://NetFPGA.org/>

-Or-

Google: "NetFPGA"



Learn More

Project summary,
videos, publications,
tutorials



Get Started

Obtain NetFPGA
hardware, download
gateway & software,
review reference
designs



Develop

Create user account,
contribute your code,
document your
project

