

NetFPGA Update at GEC4



<http://NetFPGA.org/>

NSF GENI Engineering Conference 4 (GEC4)

March 31, 2009

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Hardware and tools available for university programs thanks to grants, donations, and/or partnerships from:

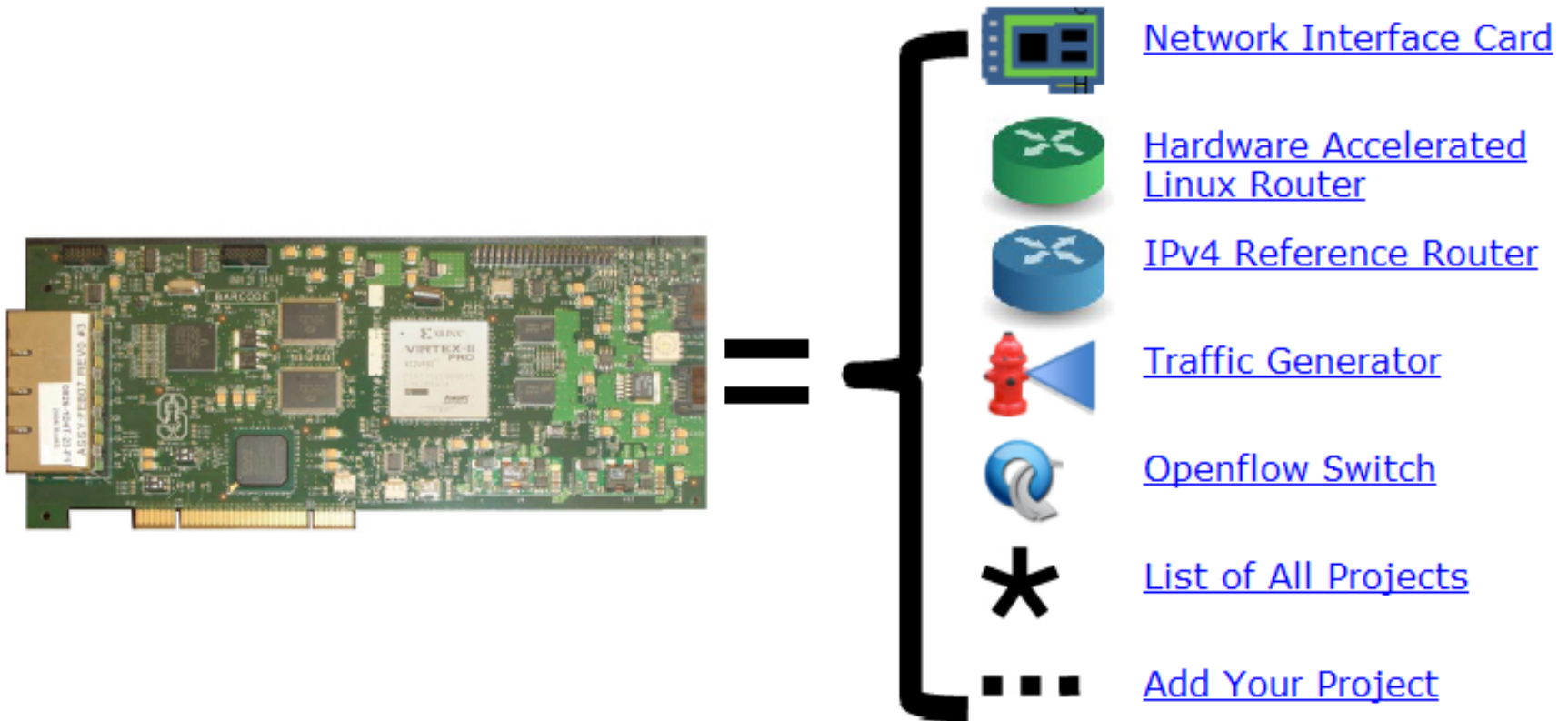


Agilent Technologies



What is the NetFPGA?

A line-rate, flexible, open networking platform for teaching and network research



Outline

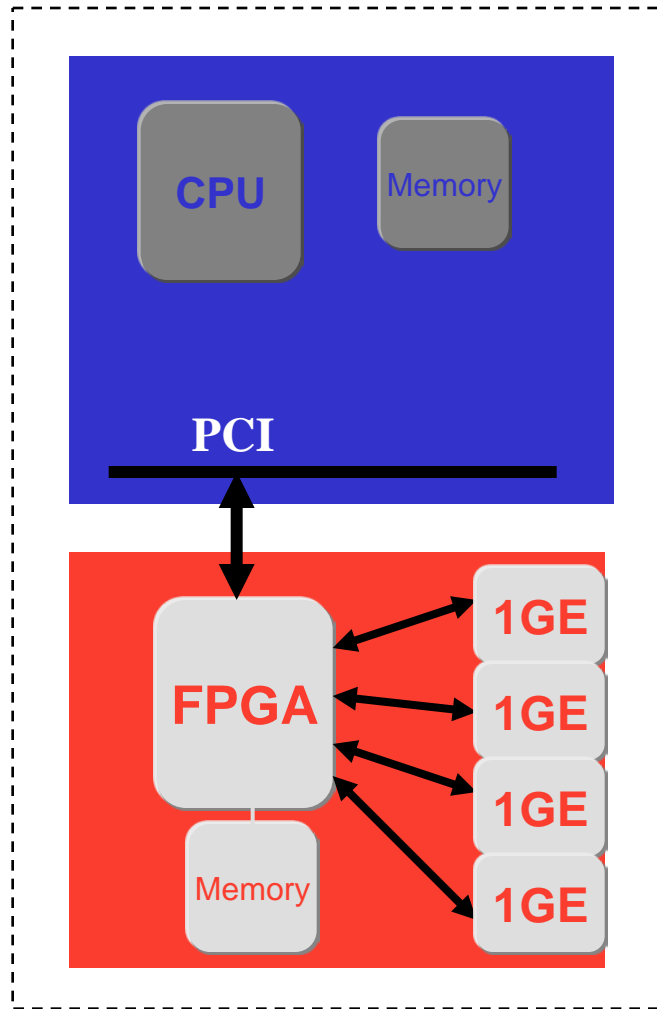
- **What is a NetFPGA system**
 - Open hardware and software
- **Why do we use reconfigurable hardware**
 - Strengths and weaknesses
- **Who uses the NetFPGA**
 - Update on worldwide deployments
- **What's new**
 - Upcoming 2.0 Release
- **Where is the NetFPGA**
 - Source code and documentation
- **How are projects contributed**
 - Regression tests
- **When is the 2009 Developers workshop**

What is a NetFPGA System

Software
running on a
standard PC

+

A hardware
accelerator
built with Field
Programmable
Gate Array
driving Gigabit
network links



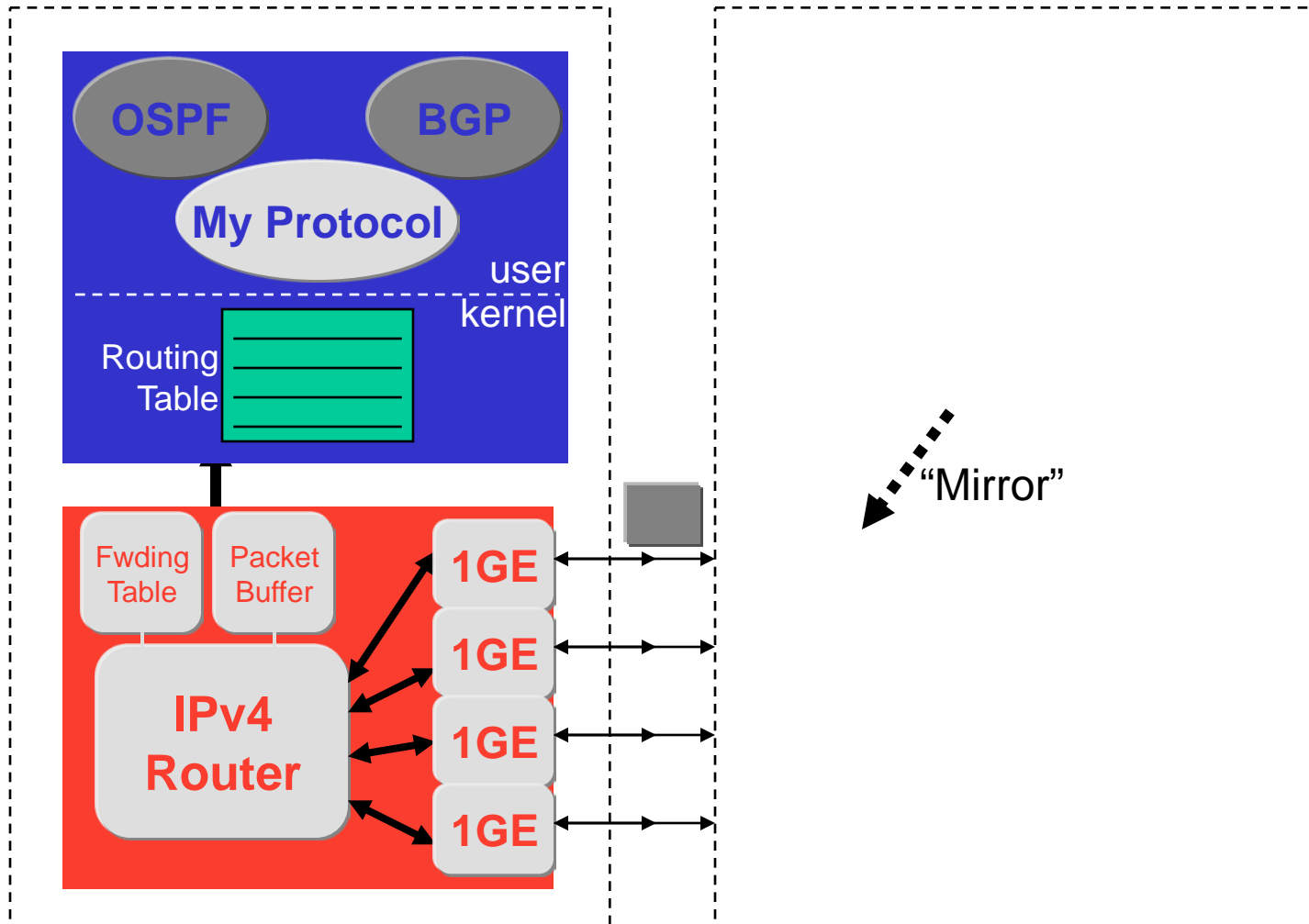
PC with NetFPGA



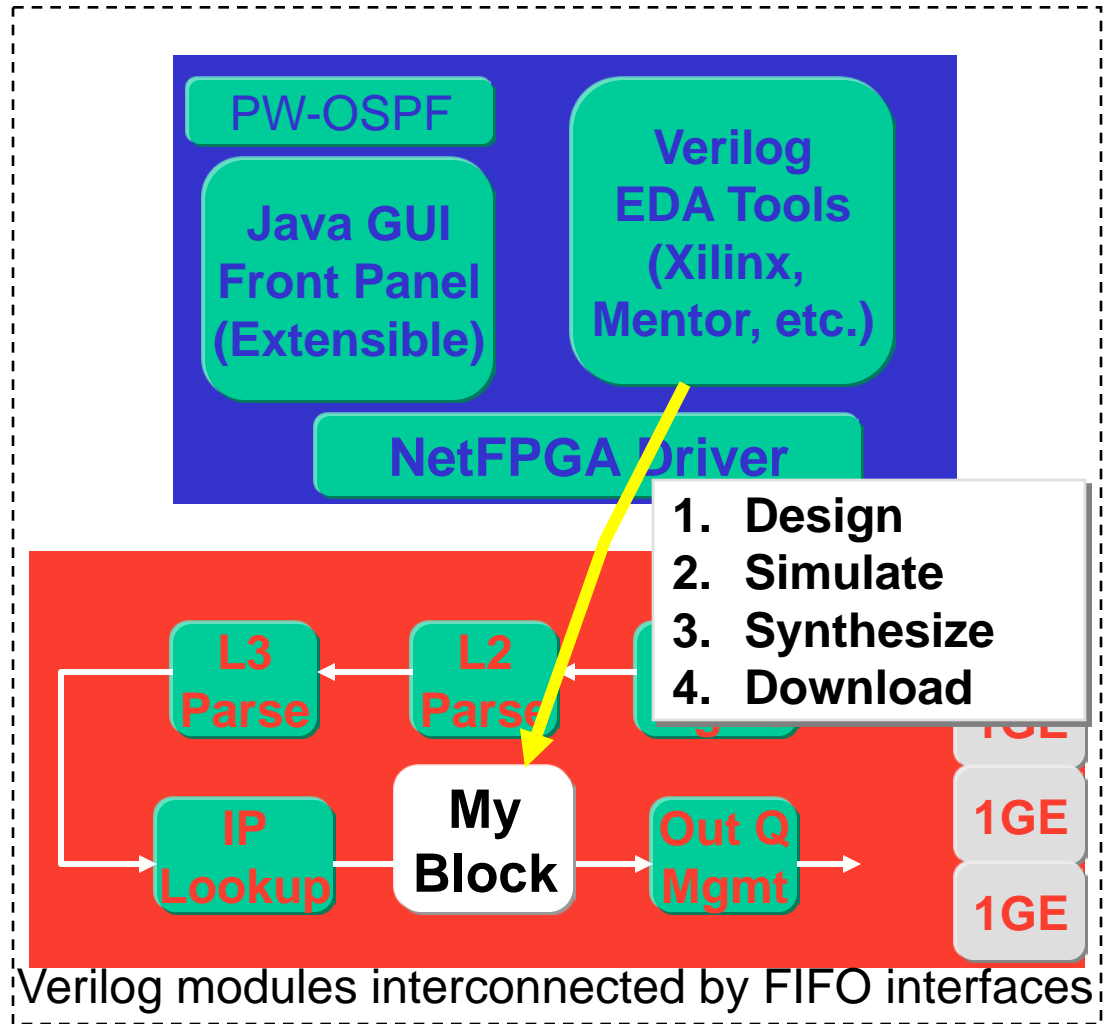
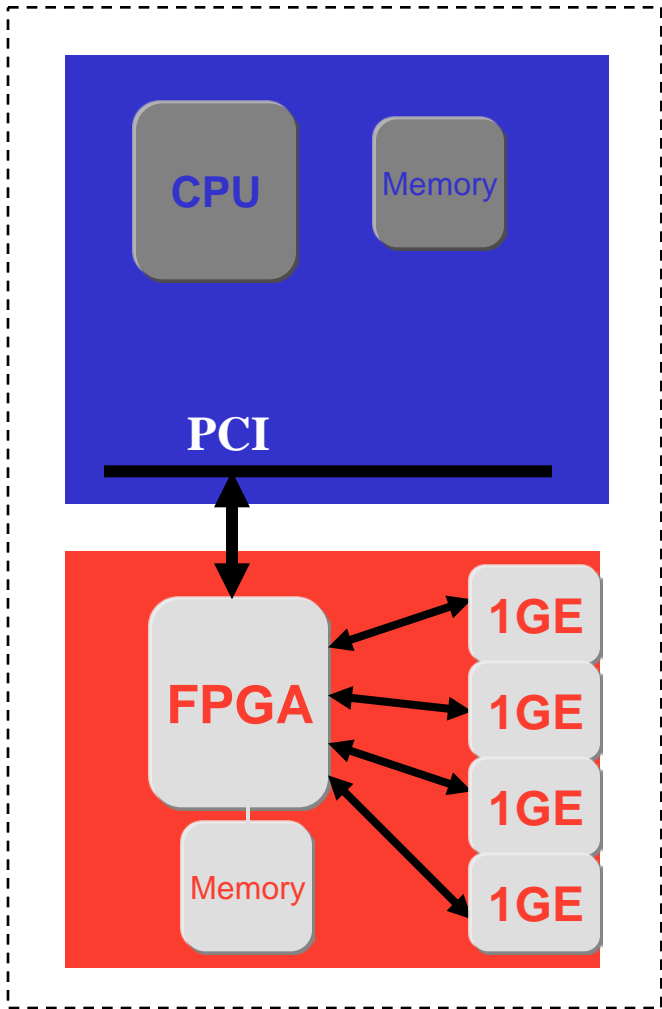
NetFPGA Board

How do I Run the Router Kit

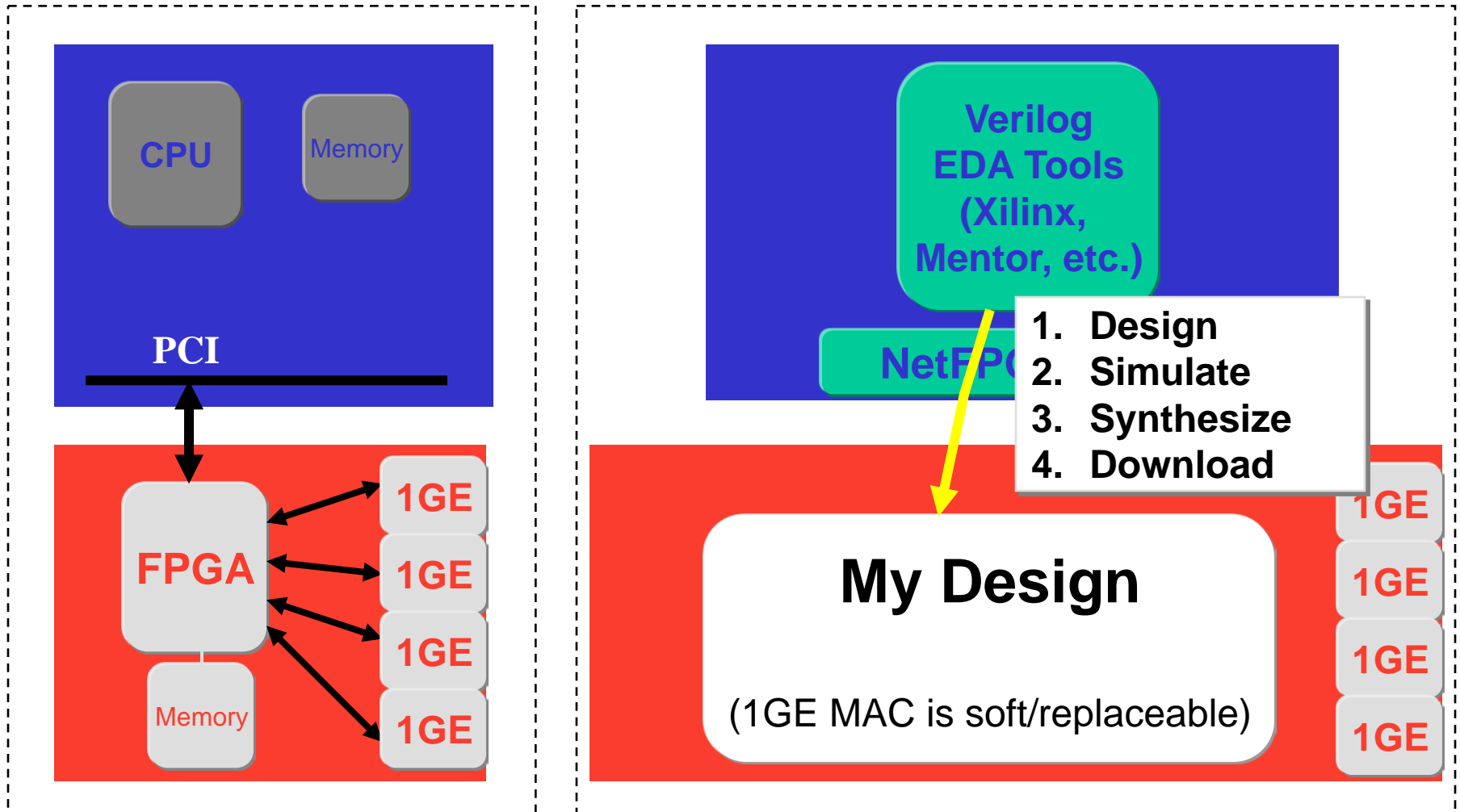
User-space development, 4x1GE line-rate forwarding



Building Modular Router Modules



How do I create new systems



Strengths of Reconfigurable Networks

- **Implement Wire-speed Processing**
 - Header Processing
 - Switching, routing, firewalls
 - Full Payload Processing
 - Content distribution and intrusion prevention
- **Enhance and create new datapath functions**
 - Monitor network flows
 - NetFlow probe
 - Control network flows
 - OpenFlow switch
 - Generate traffic
 - Traffic generator
 - Process new protocols ..

Weaknesses of Reconfiguration Nets

- **Device configuration must be secure**
 - Hackers will try to reconfigure devices
 - Competitors will try to reverse engineer applications
- **Network systems are complex**
 - Cisco routers contains 18M+ lines of code
 - Modular components needed for large systems
- **Must be power efficient**
 - FPGAs use 5-50x more power than ASIC, however
 - FPGAs use 5-50x less power than software

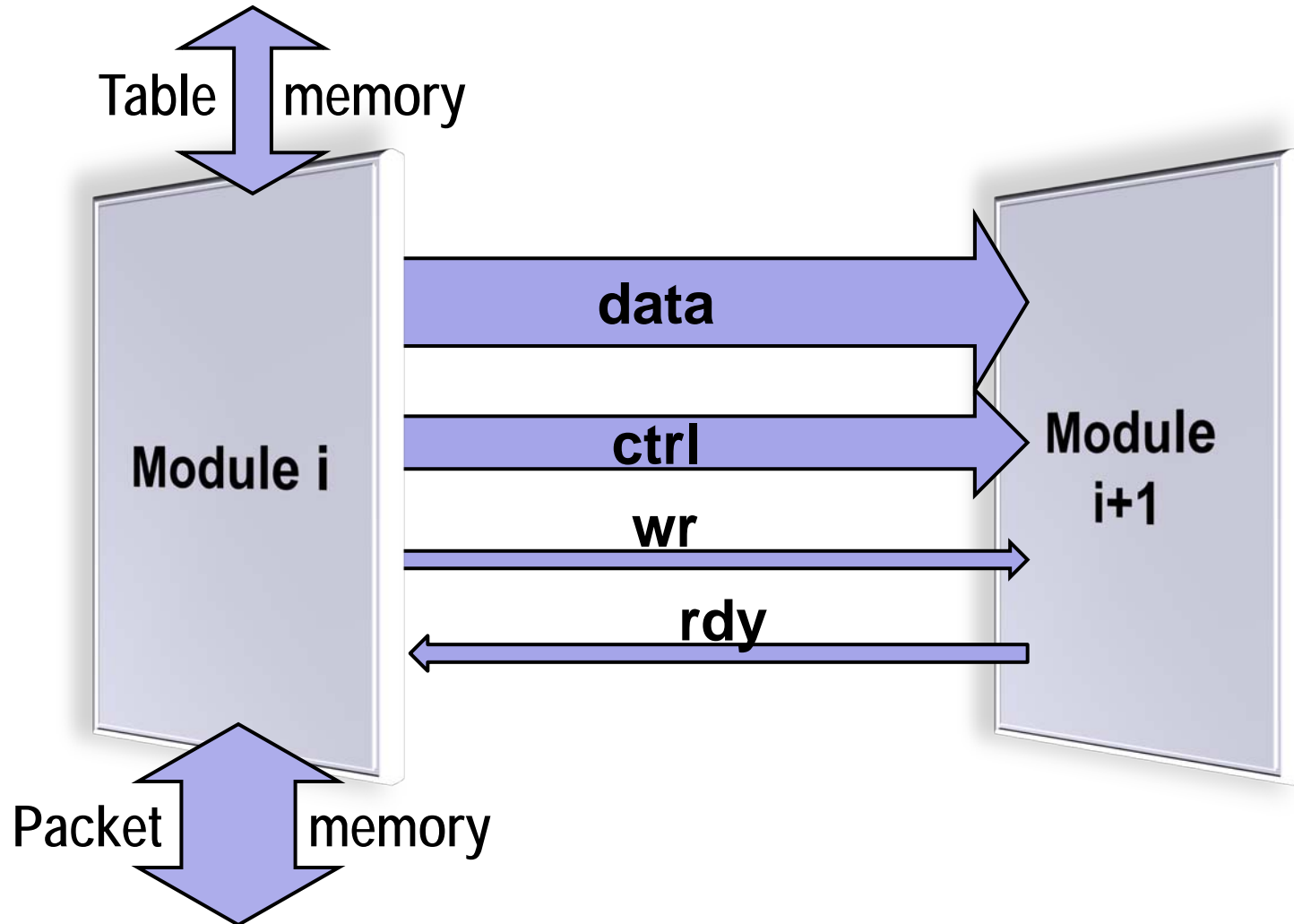
Time to Prototype New systems

- **Network systems use Multiple Languages**
 - VHDL, Verilog (Synthesizable Hardware)
 - Bluespec, Handel-C, SystemC (High-Level)
 - C, C++, Perl, PHP, Java (SW, Verification, GUIs)
- **Networks are implemented in**
 - Software:
 - Compile in seconds to minutes
 - FPGAs:
 - Synthesize in minutes to hours
 - ASICs:
 - Fabricate in months to years

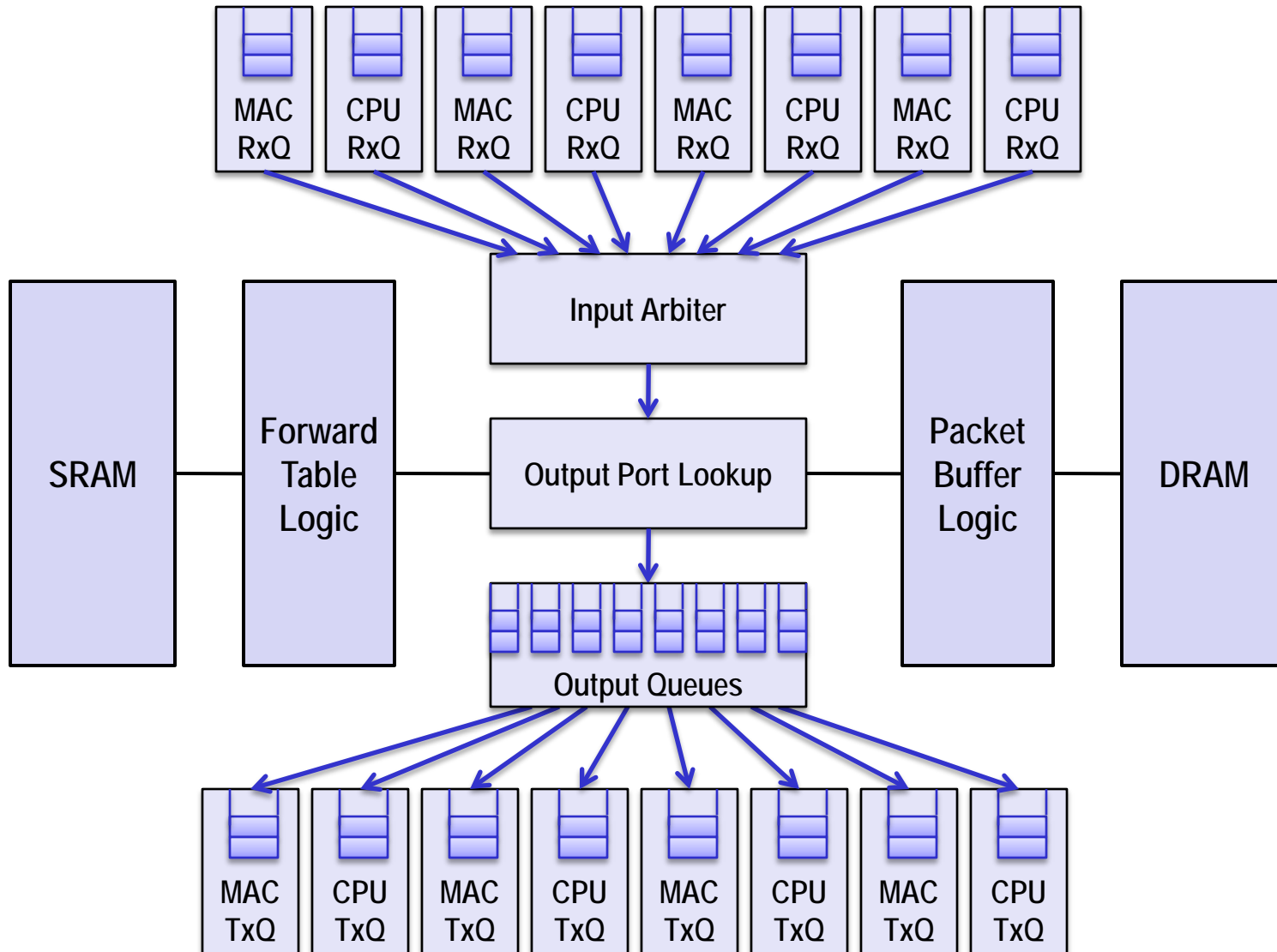
Goals for an Ideal Network Platform

- **Provide a large library of elements**
 - With modular interfaces
- **Enable systems to easily compose**
 - By combining multiple, standard elements
- **Clearly define the functionality**
 - By verification to a set of regression tests
- **Widely disseminate projects**
 - Make download as easy as using iTunes
- **Build a community of developers**
 - Organize projects
 - Document contributions
 - Respond to feedback from users
 - Encourage the community to contribute

Inter-module Communication



NetFPGA 1G Pipeline Stages



Building the NetFPGA route from the Verilog Source Code

**Using the Xilinx ISE tools to
synthesize the logic for the FPGA**

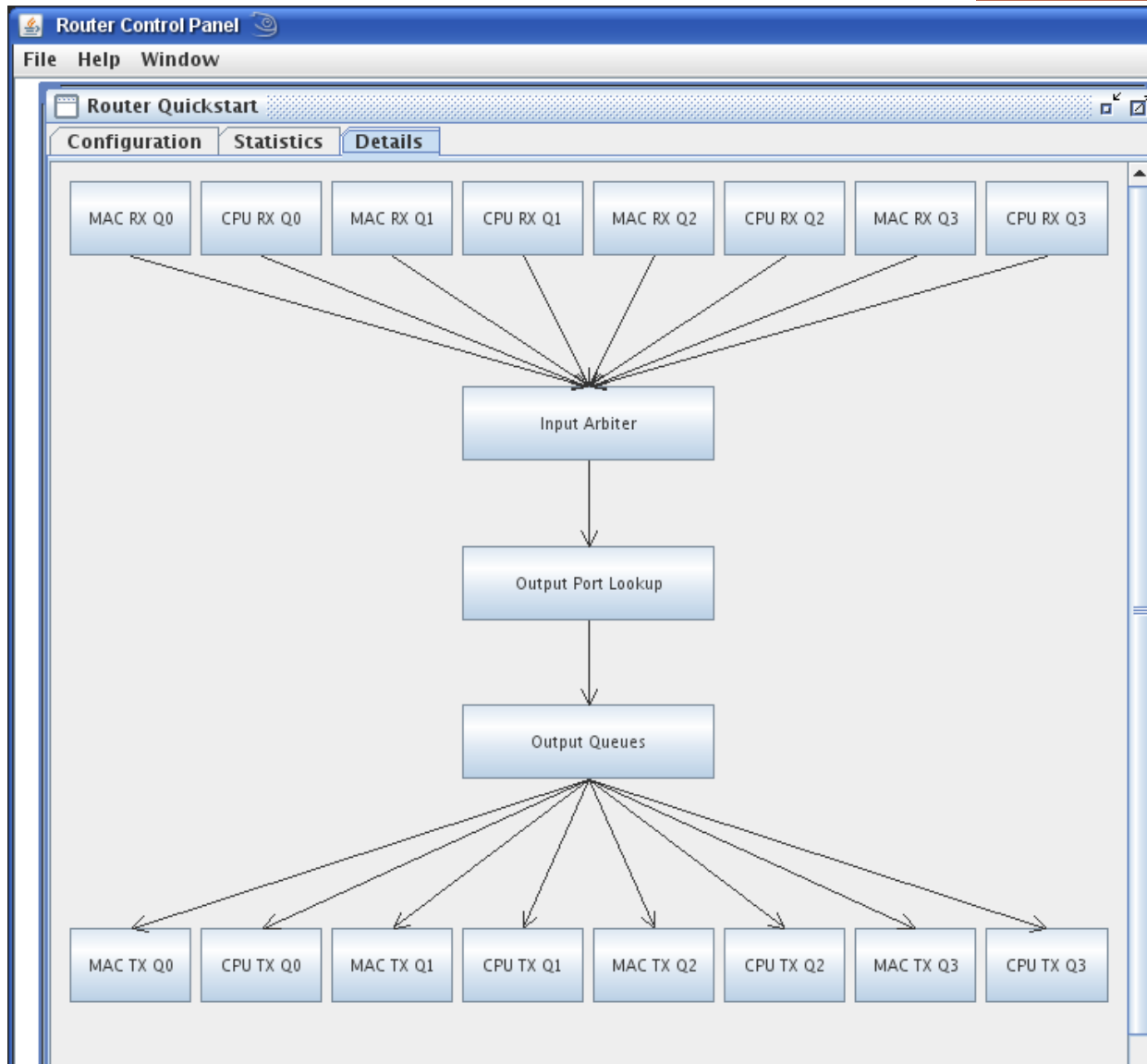
Building the NetFPGA Router

```
root@nf-test9:~/NF2/projects/tutorial_router/synth
File Edit View Terminal Tabs Help
[root@nf-test9 ~]# cd NF2/projects/tutorial_router/synth/
[root@nf-test9 synth]# make
```

```
root@nf-test9:~/NF2/projects/tutorial_router/sw
File Edit View Terminal Tabs Help
[root@nf-test9 ~]# cd NF2/projects/tutorial_router/sw/
[root@nf-test9 sw]# ./tut_router_gui.pl
```

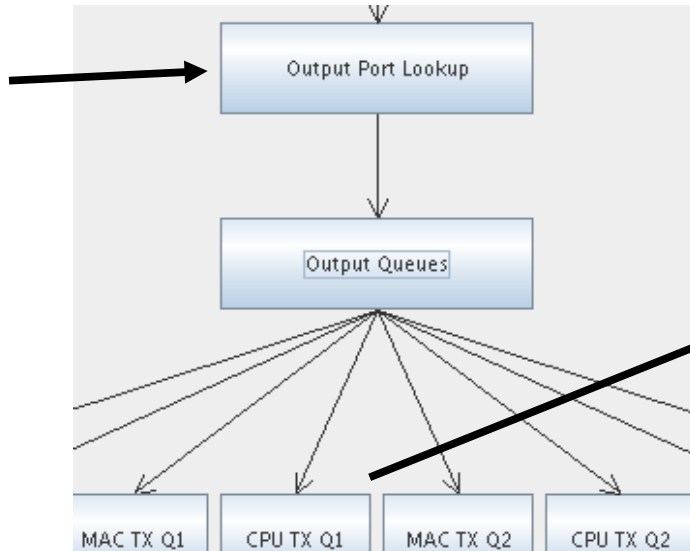
```
jnaous@jadsdesktop:~/Desktop - Shell - Konsole
Session Edit View Bookmarks Settings Help
jnaous@jadsdesktop:~/Desktop> ping 192.168.17.1
PING 192.168.17.1 (192.168.17.1) 56(84) bytes of data.
64 bytes from 192.168.17.1: icmp_seq=1 ttl=64 time=0.047 ms
64 bytes from 192.168.17.1: icmp_seq=2 ttl=64 time=0.038 ms
64 bytes from 192.168.17.1: icmp_seq=3 ttl=64 time=0.038 ms
64 bytes from 192.168.17.1: icmp_seq=4 ttl=64 time=0.044 ms
64 bytes from 192.168.17.1: icmp_seq=5 ttl=64 time=0.040 ms
64 bytes from 192.168.17.1: icmp_seq=6 ttl=64 time=0.036 ms
```

Explore the Router



Look inside the Router

Click



The screenshot shows the configuration window for Output Queues, specifically for Output Queue 4. The window includes the following settings and statistics:

- Enable:**
- Output queue size in bytes:** 512 kB (range 0 to 512 kB)
- Output queue size in packets:** no limit (range 0 to no limit)
- Buttons:** Reset Queue, Reset Stats
- Statistics:**
 - Total packets received: 0
 - Total bytes received: 0kB
 - Total packets sent: 0
 - Total bytes sent: 0kB
 - Total packets dropped: 0
 - Current Queue Occupancy (packets): 0
 - Current Queue Occupancy (bytes): 0kB
- Graphs:**
 - Packet Drops due to Full Queue:** Number of dropped packets vs. time. Legend: Packets dropped.
 - Queue Occupancy (bytes):** Queue Occupancy (kB) vs. time. Legend: Bytes used.
 - Queue Occupancy (pkts):** Queue Occupancy vs. time. Legend: Num Packets in Queue.

Why do we use the NetFPGA

- **To run laboratory courses on network routing**
 - Professors teach courses (CS344, Workshops, ..)
- **To teach students how to build real Internet routers**
 - Train students to build routers (Cisco, Juniper, Huawei, ..)
- **To research how new features in the network**
 - Build network services for data centers (Google, UCSD..)
- **To prototype systems with live traffic**
 - That Buffer measurement (while maintaining throughput, ..)
- **To help hardware vendors understand device requirements**
 - Use of hardware (Xilinx, Micron, Cypress, Broadcom, ..)

Where are NetFPGAs?

- Over 500 users with ~1,000 cards deployed
- Deployed in ~120 universities in 17 Countries



Photos from NetFPGA Tutorials



SIGCOMM - Seattle, Washington, USA



Beijing, China



SIGMETRICS - San Diego, California, USA



EuroSys - Glasgow, Scotland, U.K.



Bangalore, India

<http://netfpga.org/pastevents.php> and <http://netfpga.org/upcomingevents.php>

NetFPGA Systems

- **PCs assembled from parts**
 - Integrates into standard PC
- **Pre-built systems available**
 - From 3rd Party Vendor
- **Details are in the Guide**
 - <http://netfpga.org/static/guide.html>



Rackmount NetFPGA Servers



**2U Server
(Dell 2950)**



**NetFPGA inserts in
PCI or PCI-X slot**

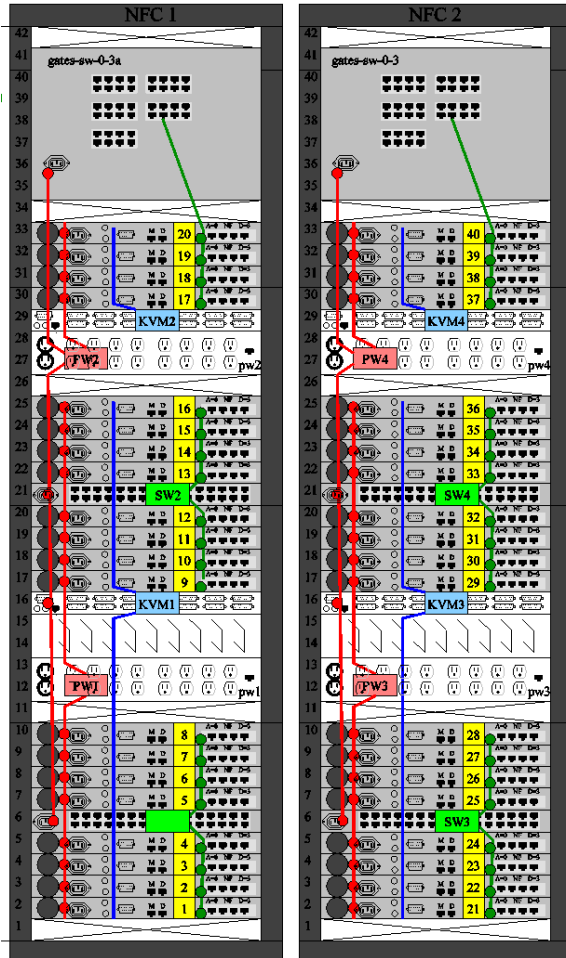


**1U Server
(Accent Technology, Inc)**

Thanks: Brian Cashman for providing machine

Stanford NetFPGA Cluster

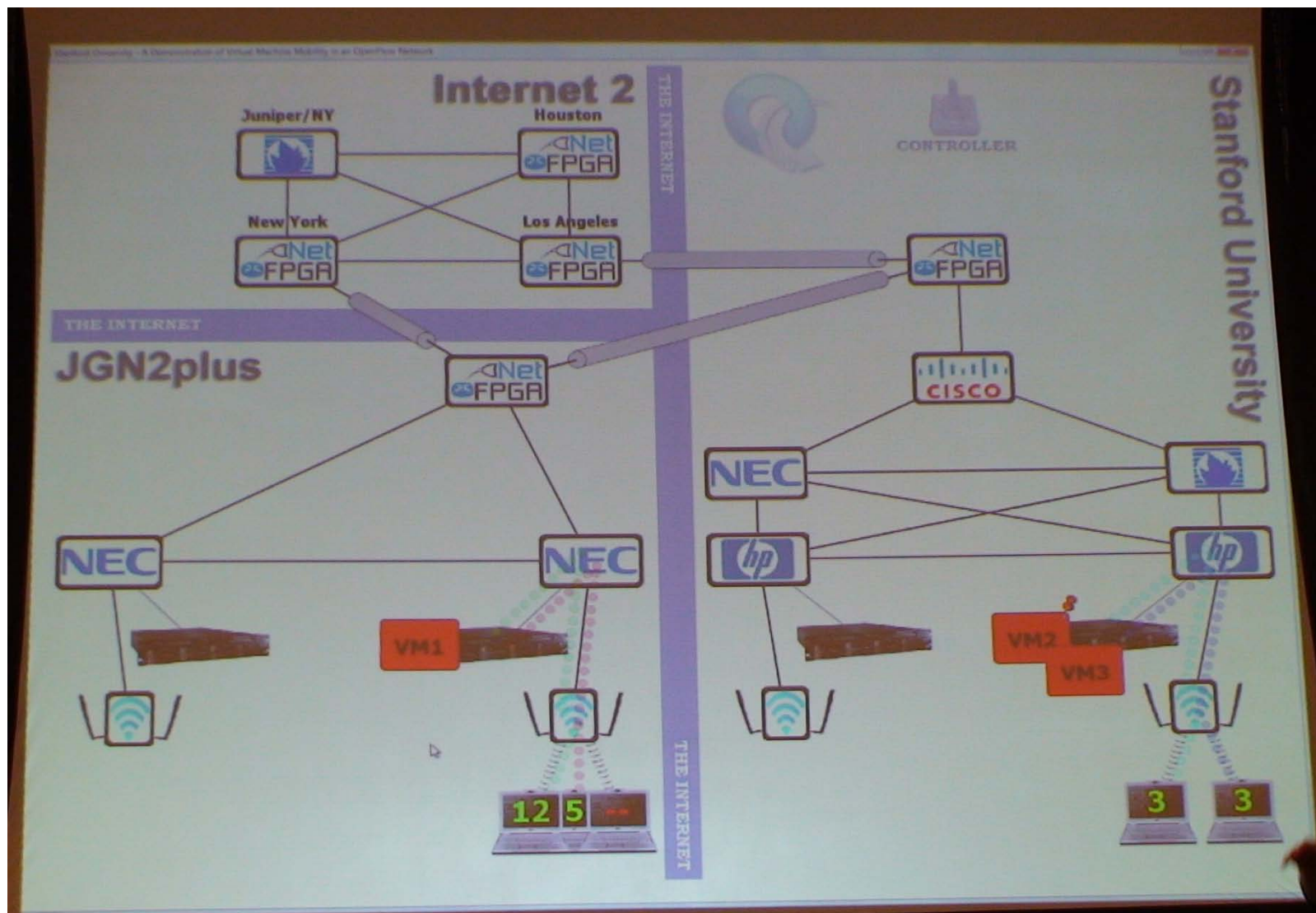
Stanford NetFPGA Cluster (NFC)
Internetconnect-side View



Statistics

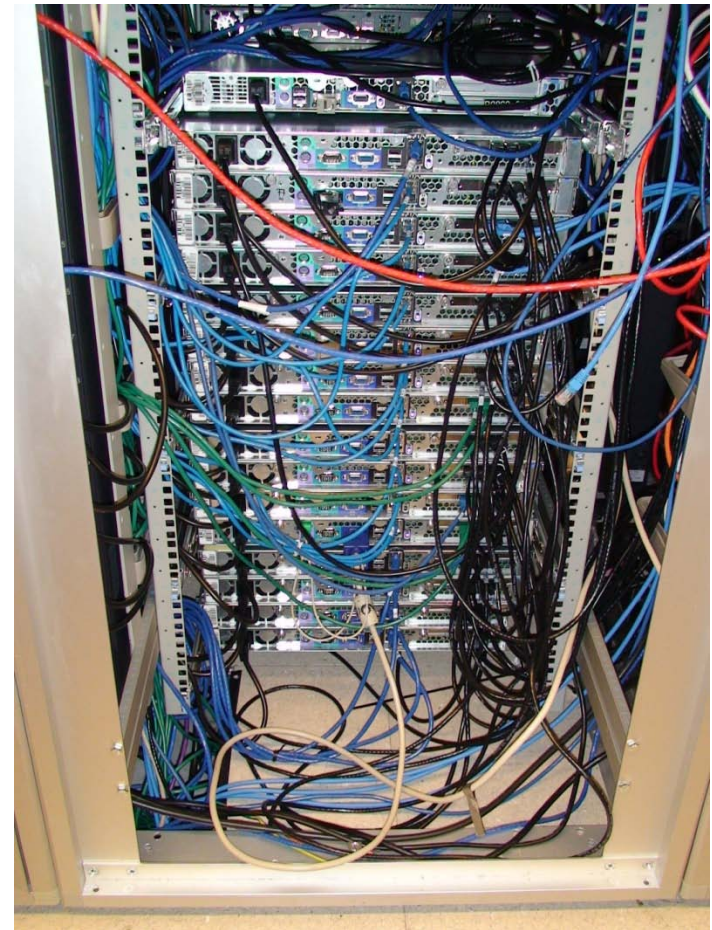
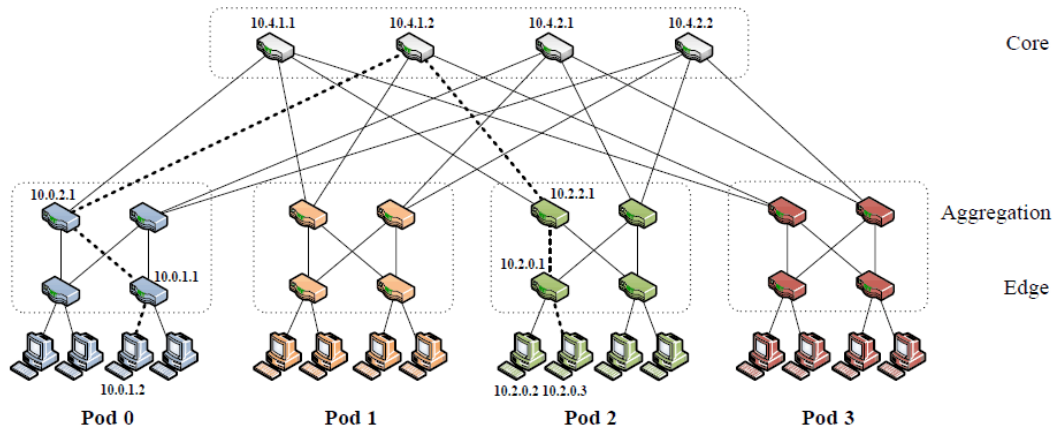
- Rack of 40
 - 1U PCs
 - NetFPGAs
- Manged
 - Power,
 - Console
 - VLANs
- Provides 160 Gbps of full line-rate processing bandwidth

NetFPGAs in the Internet 2 & Japan



From GENI Engineering Conference – Oct 2008

UCSD-NetFPGA Cluster



Preview of Upcoming 2.0 Release

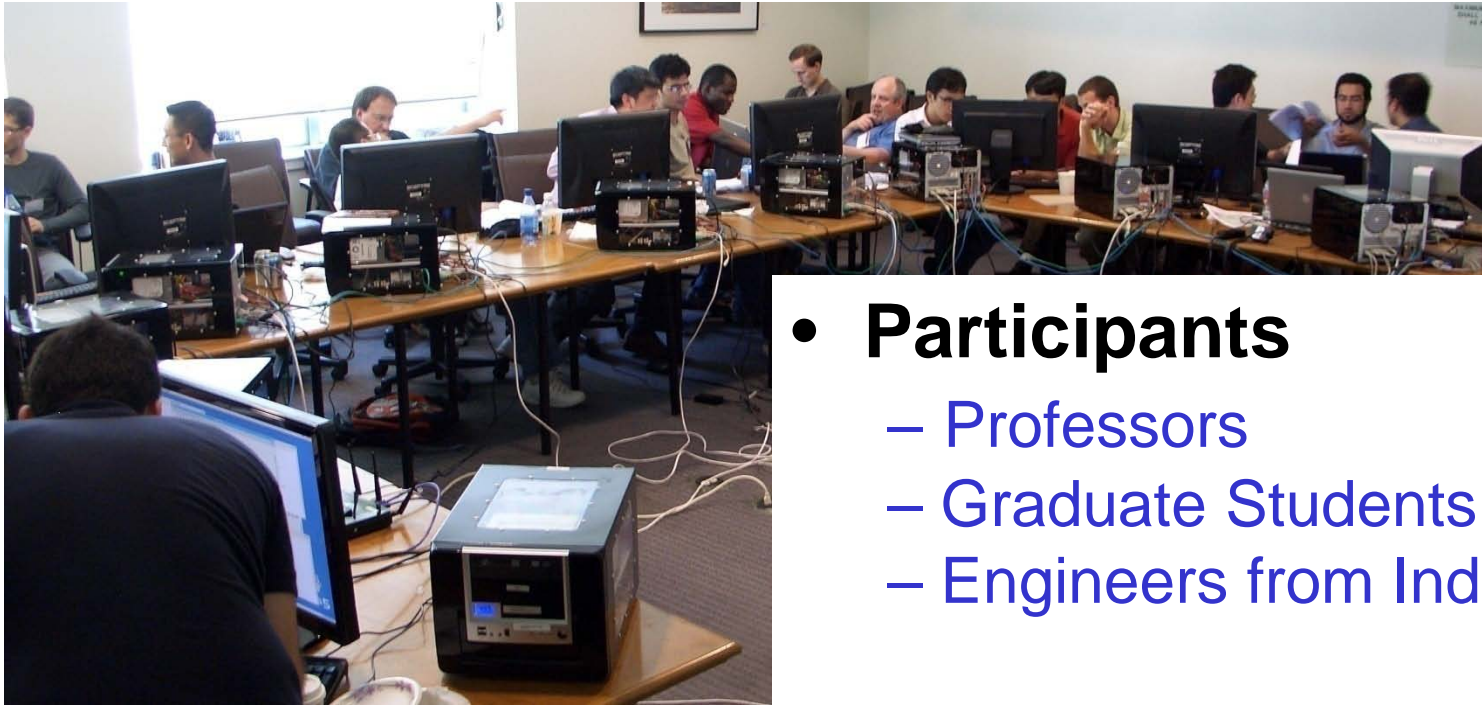
- **Modular Registers**
 - Shares
 - Project registers specified by XML list
 - Joined together at build time

- **Packet buffering in DRAM**
 - Deep buffer
 -

Conclusions

- **NetFPGA Provides**
 - Open-source, hardware-accelerated Packet Processing
 - Modular interfaces arranged in reference pipeline
 - Extensible platform for packet processing
- **NetFPGA Reference Code Provides**
 - Large library of core packet processing functions
 - Scripts and GUIs for simulation and system operation
 - Set of Projects for download from repository
- **The NetFPGA Community of Developers use**
 - Well defined functionality defined by regression tests
 - Blogs that organize projects
 - Wiki pages that Document contributions
 - Forum for discussion of feedback from users

NetFPGA 2008 Summer Camp



- **Participants**

- Professors
- Graduate Students
- Engineers from Industry

- **Format : One week event at Stanford**

- 2.5 Days of Training on the reference router
- 2 Days to work on projects
- Final Projects presented on Friday Afternoon

NetFPGA Developers Workshop

August 13-14, 2009 at Stanford University

- You already know that the NetFPGA implements a Gigabit NIC, a hardware-accelerated Internet router, a traffic generator, an OpenFlow switch, a NetFlow probe and more. What else can it do? We invite you, our worldwide NetFPGA Developers, to show off your project. Submit a paper to describe your project, prepare a demo, and come to Stanford in August to demonstrate your work!

- **Papers Due:**

- April 20, 2009

- **Workshop Date:**

- Aug. 13-14, 2009

- **Paper Format:**

- 4-8 page, ACM-style

- **Demonstrations:**

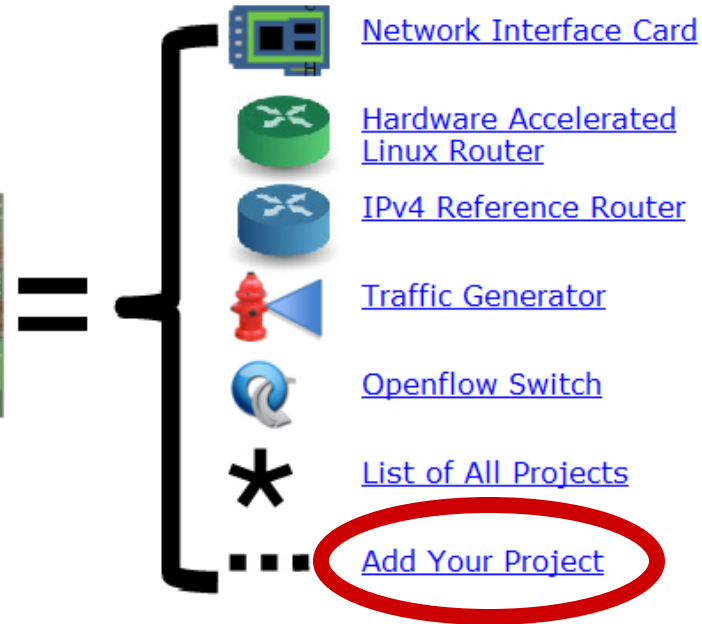
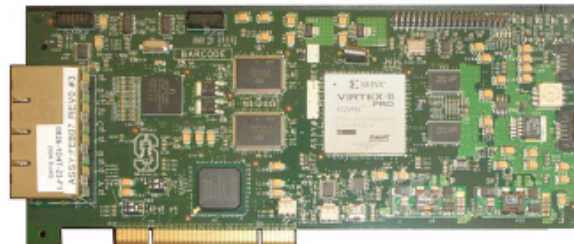
- Run on NetFPGA(s)

- **Program Chairs:**

- John W. Lockwood (Stanford University)
- Andrew W. Moore (Cambridge University)

- **Full Details**


- <http://NetFPGA.org/DevWorkshop>



“What have you built with your NetFPGA?”

Additional Slides

Need Help? – See Discussion Forums

 **NetFPGA Forum**

User Name Remember Me?

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Welcome to the NetFPGA Forum.

If this is your first visit, be sure to check out the [FAQ](#) by clicking the link above. You may have to [register](#) before you can post: click the register link above to proceed. To start viewing messages, select the forum that you want to visit from the selection below.

Forum	Last Post	Threads	Posts
General NetFPGA discussion 			
A forum dedicated to general NetFPGA discussion, including installation, setup and usage.			
 General Discussion General discussion forum about the NetFPGA platform	 computer freezes when I... by sumeet23 02-06-2009 10:49 PM 	54	209
 Installation and Setup (3 Viewing) This forum should be used for discussion of installation and setup of the NetFPGA system.	 "download failed" when... by Abhishek 02-07-2009 12:05 AM 	39	179
 Forum requests/queries Forum to request new forums/query existing forums.	 Increase the flexibility in... by gac1 01-12-2009 06:57 PM 	2	3
Projects 			
Forums dedicated to specific NetFPGA projects			
 Packet Generator Discussions related to the packet generator	 Feature requests by grq 01-16-2009 09:56 PM 	7	34

NetFPGA Hardware in North America

Locations of Deployed NetFPGA Hardware

USA - Jan 2009



NetFPGA Hardware in Europe

Locations of Deployed NetFPGA Hardware

EU - Jan 2009



NetFPGA Hardware in Asia

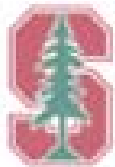
Locations of Deployed NetFPGA Hardware



China, Korea, Japan, Taiwan - Jan 2009

Acknowledgements

Support for the NetFPGA project is provided by the following organizations, companies, and institutions



Agilent Technologies



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Learn more About the NetFPGA

<http://NetFPGA.org/>

-or-

Google: "NetFPGA"



Learn More

Project summary,
videos, publications,
tutorials



Get Started

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hardware, download
gateway & software,
review reference
designs



Develop

Create user account,
contribute your code,
document your
project