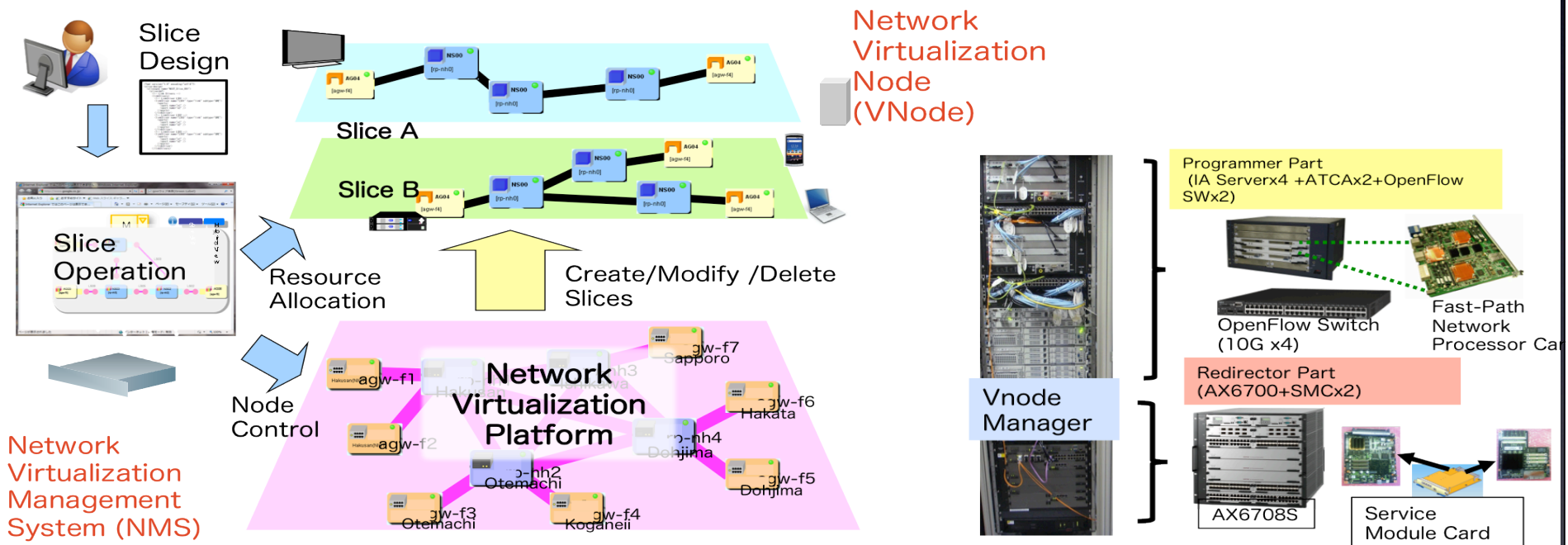


International Collaborations:
Federated VNode / GENI
Packet Cache Demonstration

Aki Nakao
University of Tokyo
2012/10/24

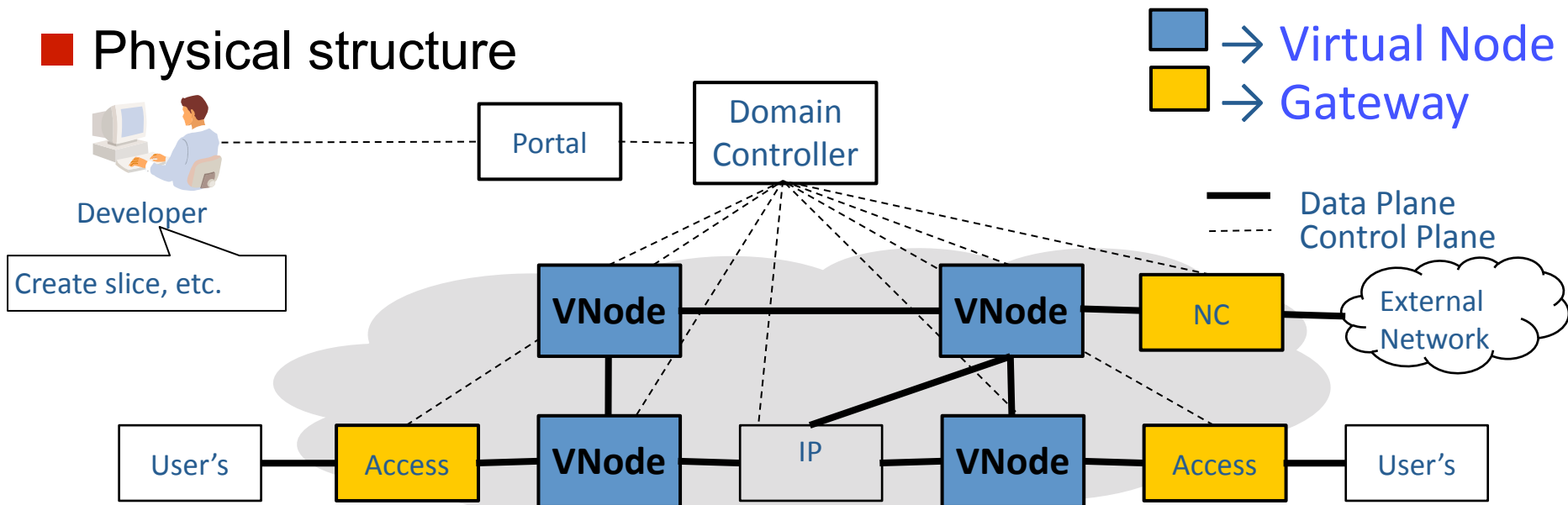
VNode Project in Japan

- VNode Infrastructure Enables **Deeply Programmable Network**
(Project Leader: Aki Nakao)
- 2008-2010 Collaborative Research (NICT/Utokyo/NTT/NEC/Hitachi/Fujitsu)
- 2011-2014 Collaborative Research (Utokyo/NTT/NEC/Hitachi/Fujitsu/KDDI)



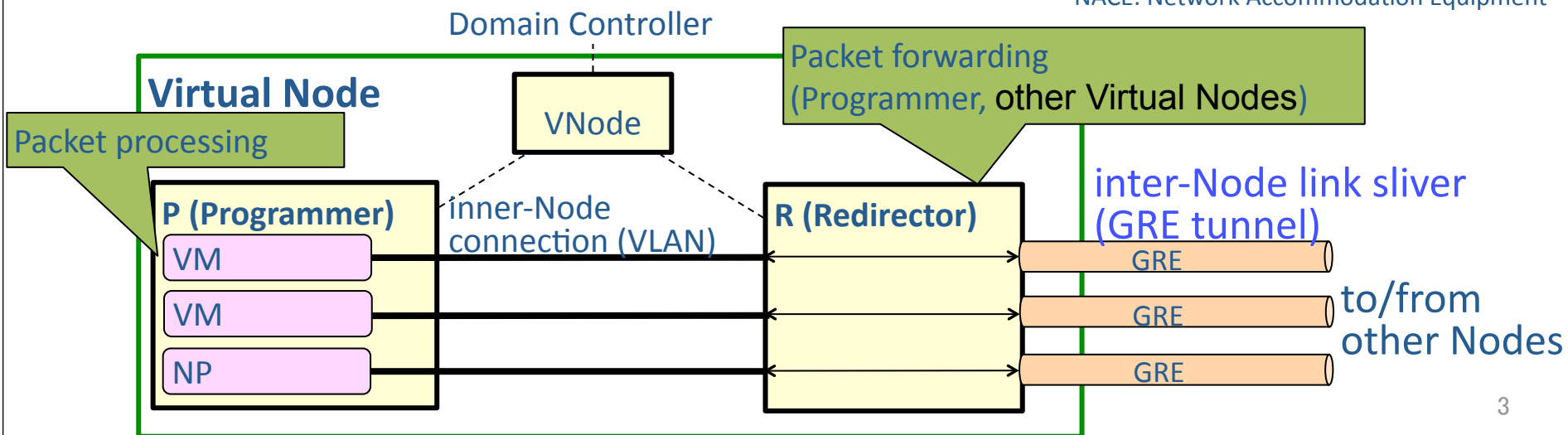
VNode architecture

Physical structure



Detailed structure of Virtual Node

VM: Virtual Machine
 NP: Network Processor
 GRE: Generic Routing Encapsulation
 NACE: Network Accommodation Equipment

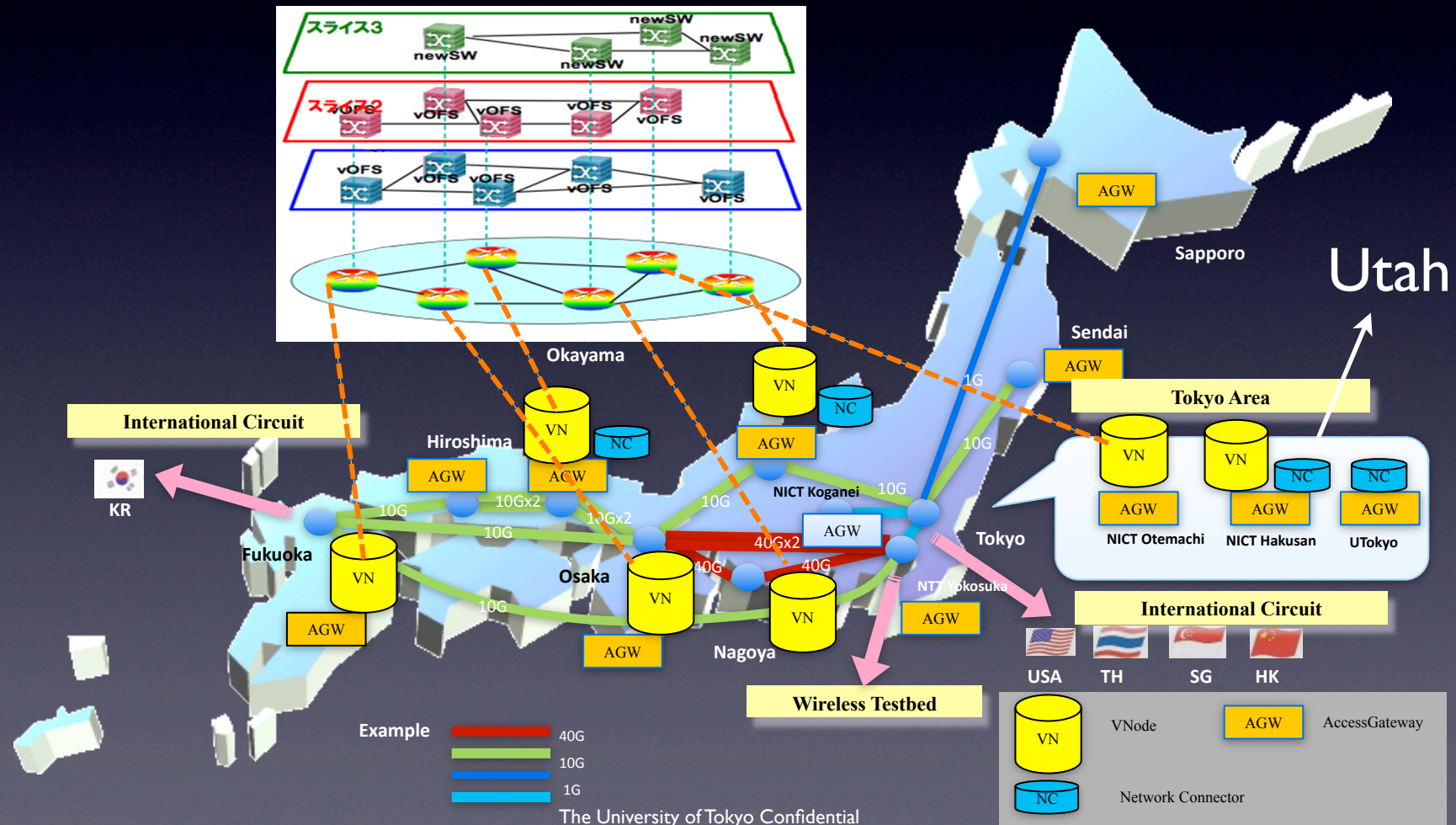


VNode Infrastructure



VNode Infrastructure (extended to US!)

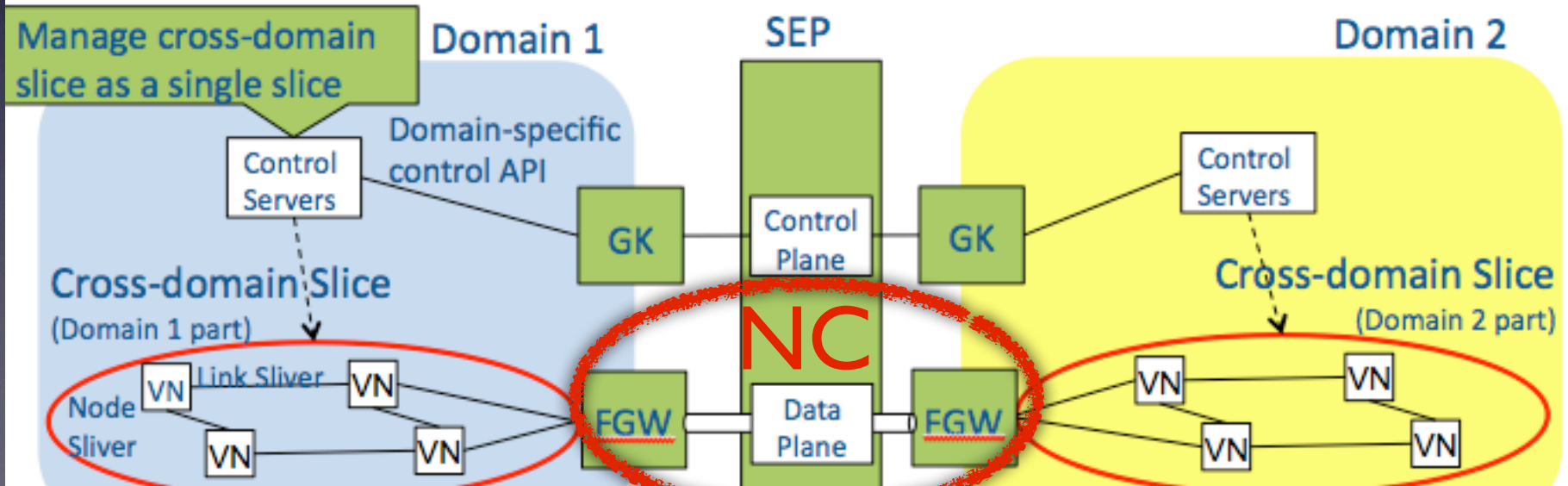
- 7 VNodes, 4 Network Connectors, 11 Access Gateways
- Deep Programmability for Experimenting with Arbitrary Protocols (Non-)
- **Slice-Around-The-World Project (A VNode in U of Utah)**



C/D Plane Federation

1. Basic Federation Architecture

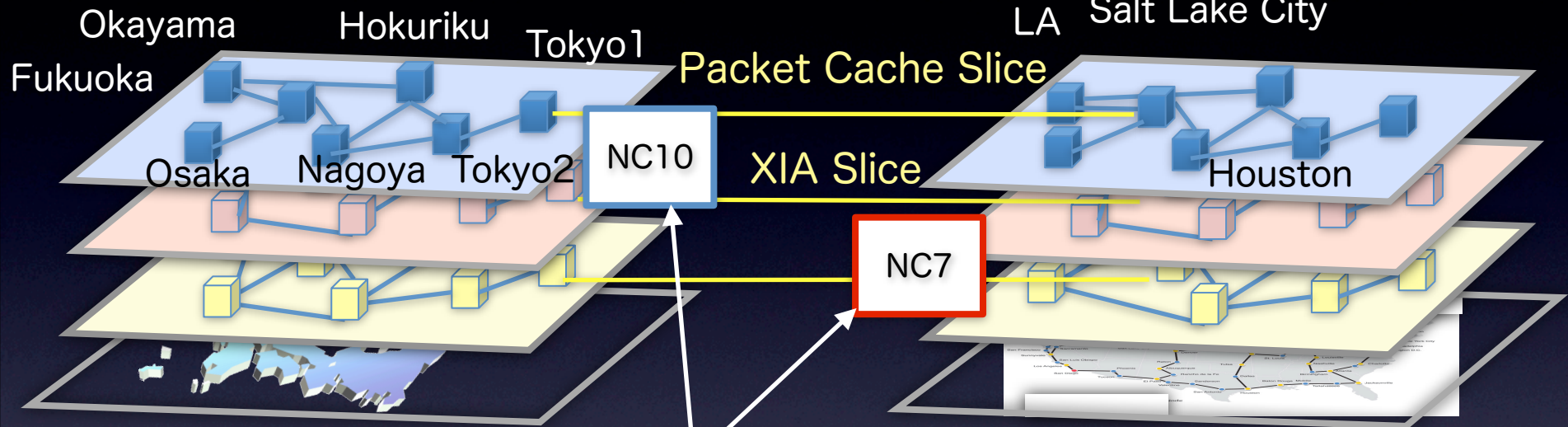
- General federation architecture between different virtualization platforms (different concept, API)
- Gatekeeper (GK) / Federation Gateway (FGW)
 - Translate API / data to common API / packet format
- Slice Exchange Point (SEP) Command sequence, Slice expiration, etc.
 - Bridge commands, control frameworks, policies etc.



Data Plane Federation (VNode / GENI)

VNode

ProtoGENI

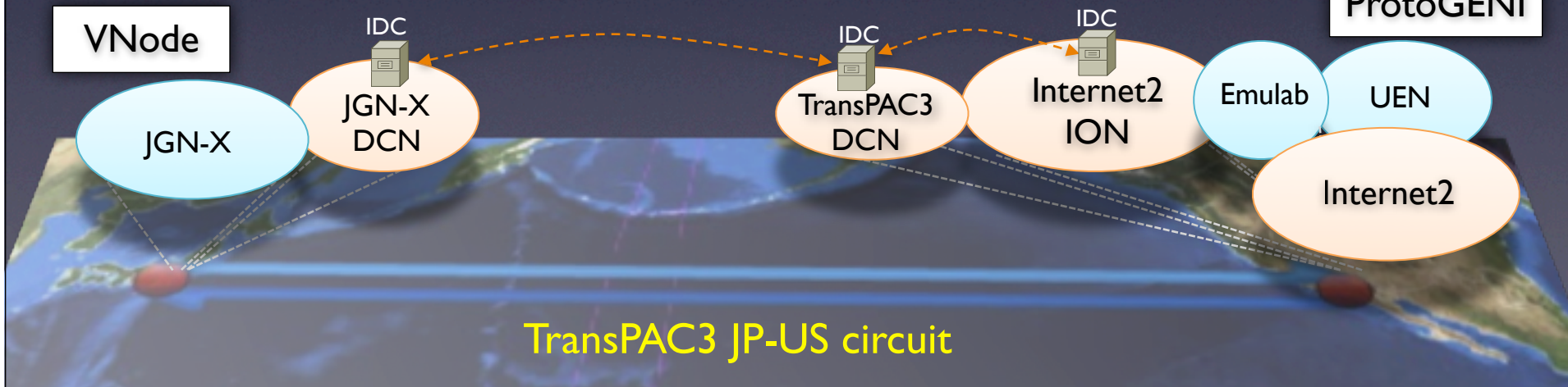


JGN-X

VNode Front-End (Network Connector)

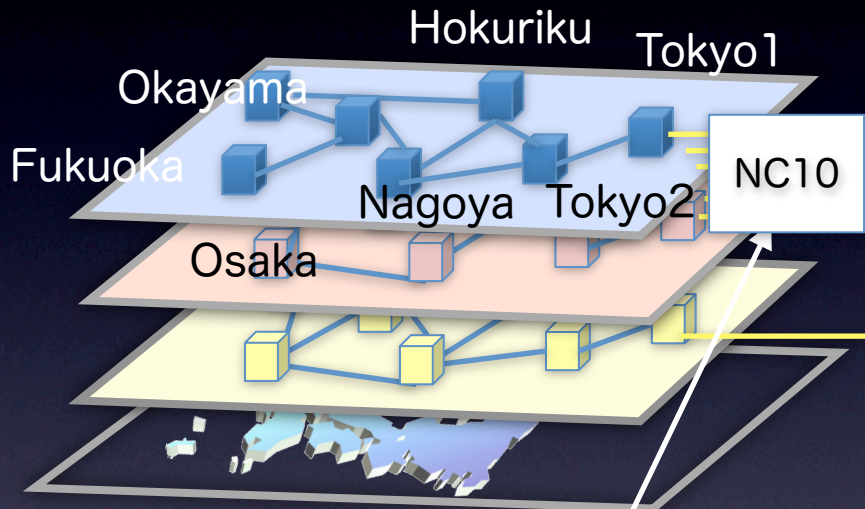
I2

ProtoGENI



VNode

Not Scalable for # of Slices
(Allocating **as many VLANs as slices** over Pacific Ocean)

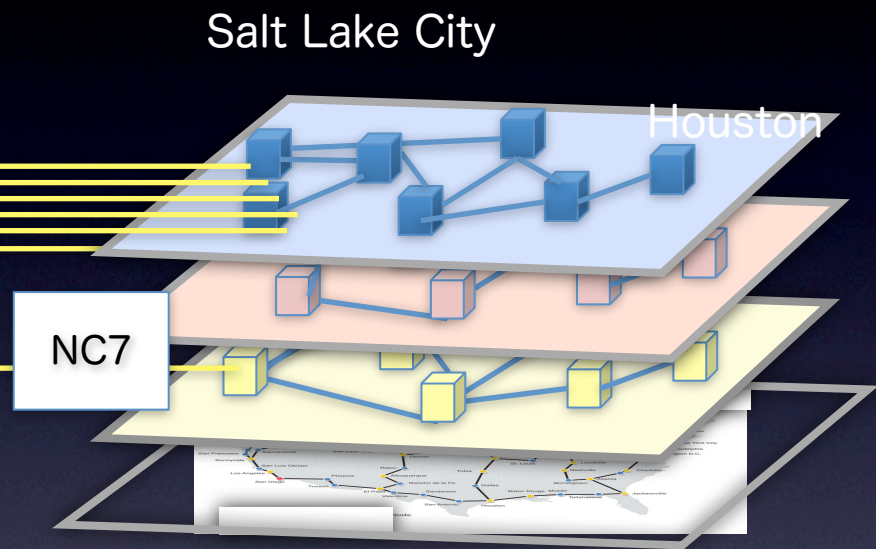


JGN-X

VNode Front-End

GRE <-> VLAN ID

ProtoGENI

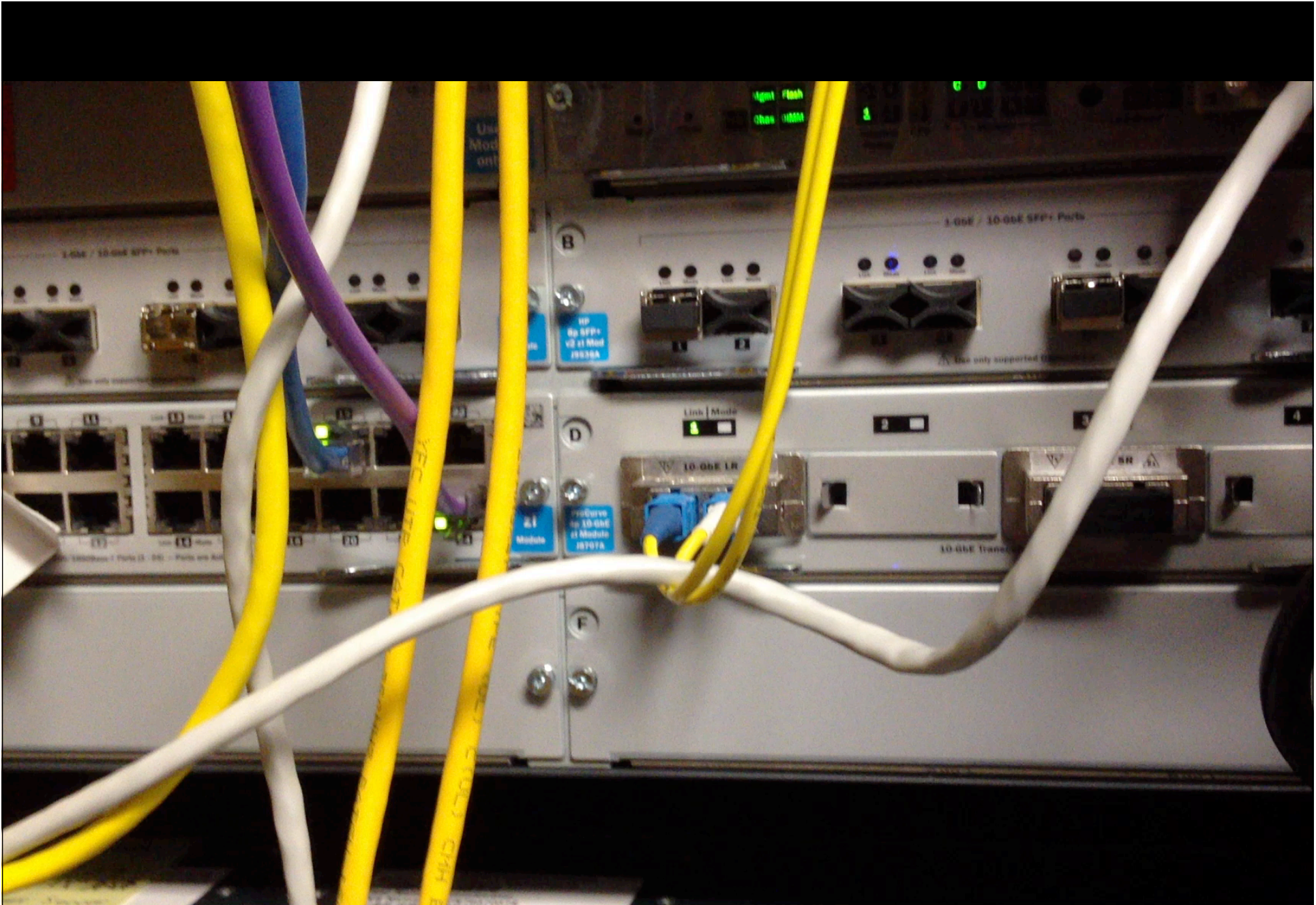


12

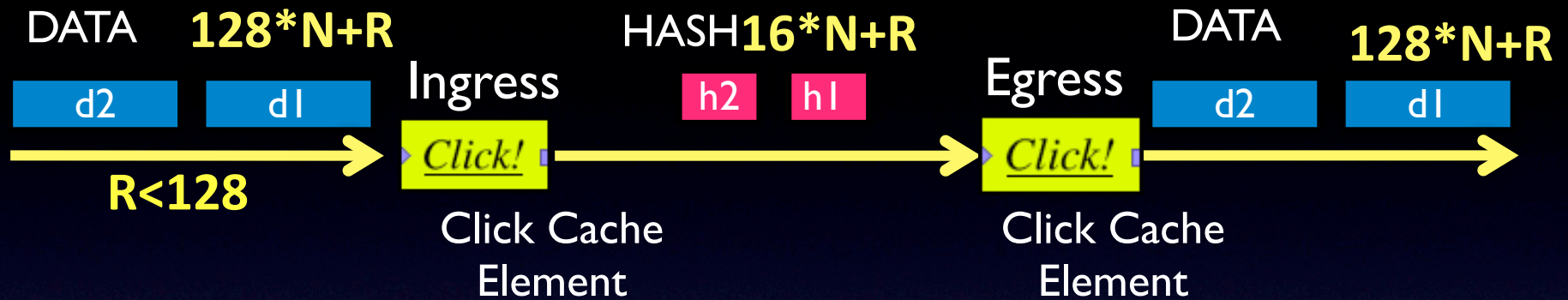
Scalable for # of Slices
(Allocating **as a single VLAN** over Pacific Ocean)

VNode in instGENI Rack@Emulab

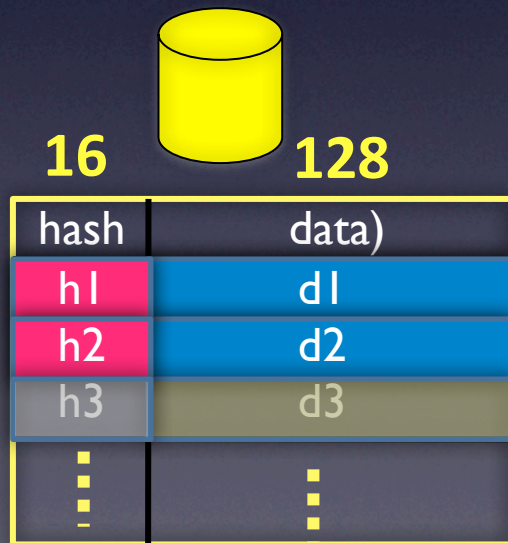




Packet Cache

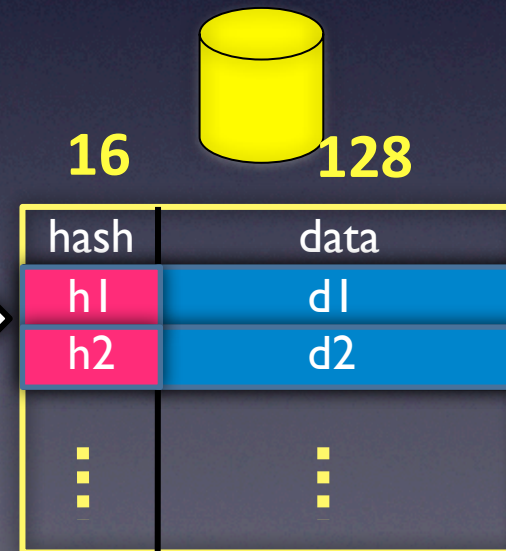


Ingress Cache

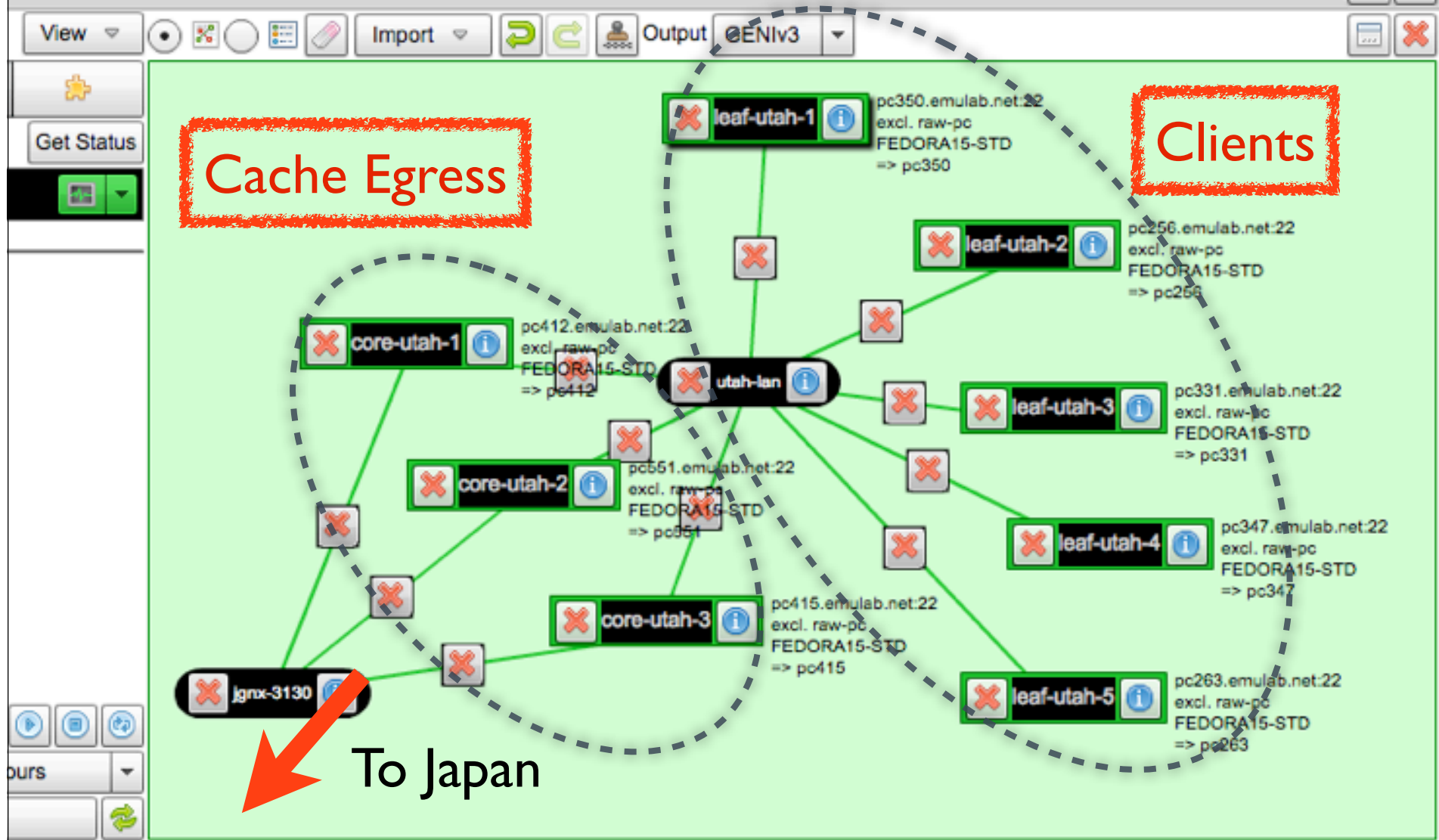


Data Sync.

Egress Cache



Packet Cache Slice Configuration in ProtoGENI



Packet Cache Slice Configuration in VNode

File Edit View History Bookmarks Tools Help

http://192.168.40.53/gui/Developer/SliceListView.do

Most Visited Getting Started Latest Headlines

Developer : Slice Operation

Do you want Firefox to remember the password for "utokyo_dev" on http://192.168.40.53?

Remember

Never for This Site

Not Now

Slice Operation

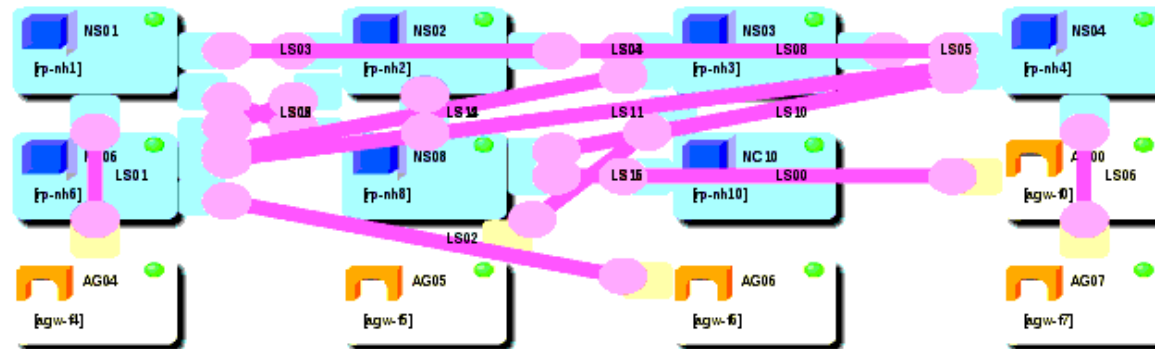
Slice121001_ut



Slice View

Hybrid View

x1



Operation

Egress Inlb

IPsec SA

User

Statistics

Sliver Status

Property

Alive Status

History

Update



Initial

Created

Bound

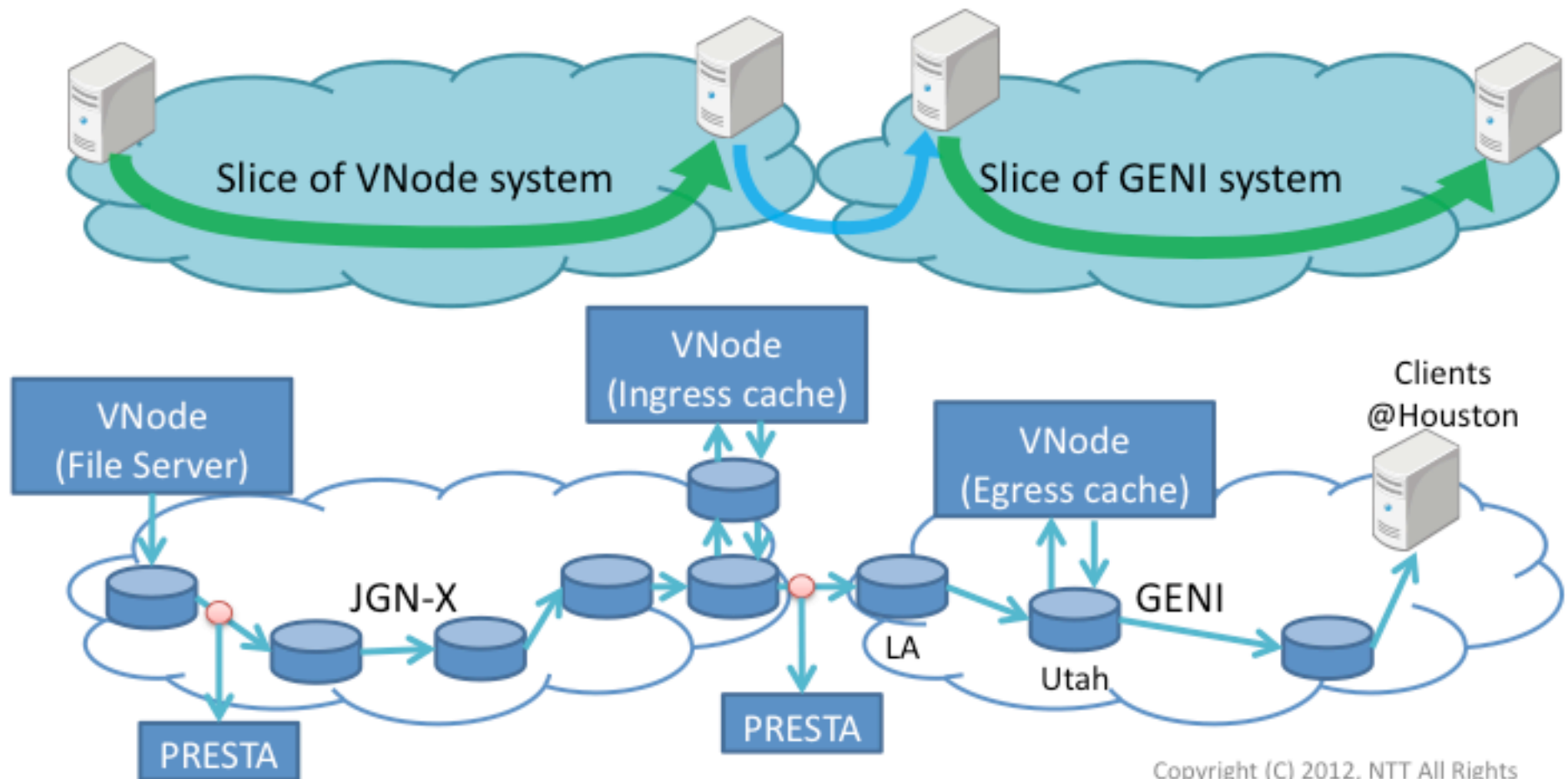
Run

Started



Transferring data from 192.168.40.53...

Demonstration NW configuration

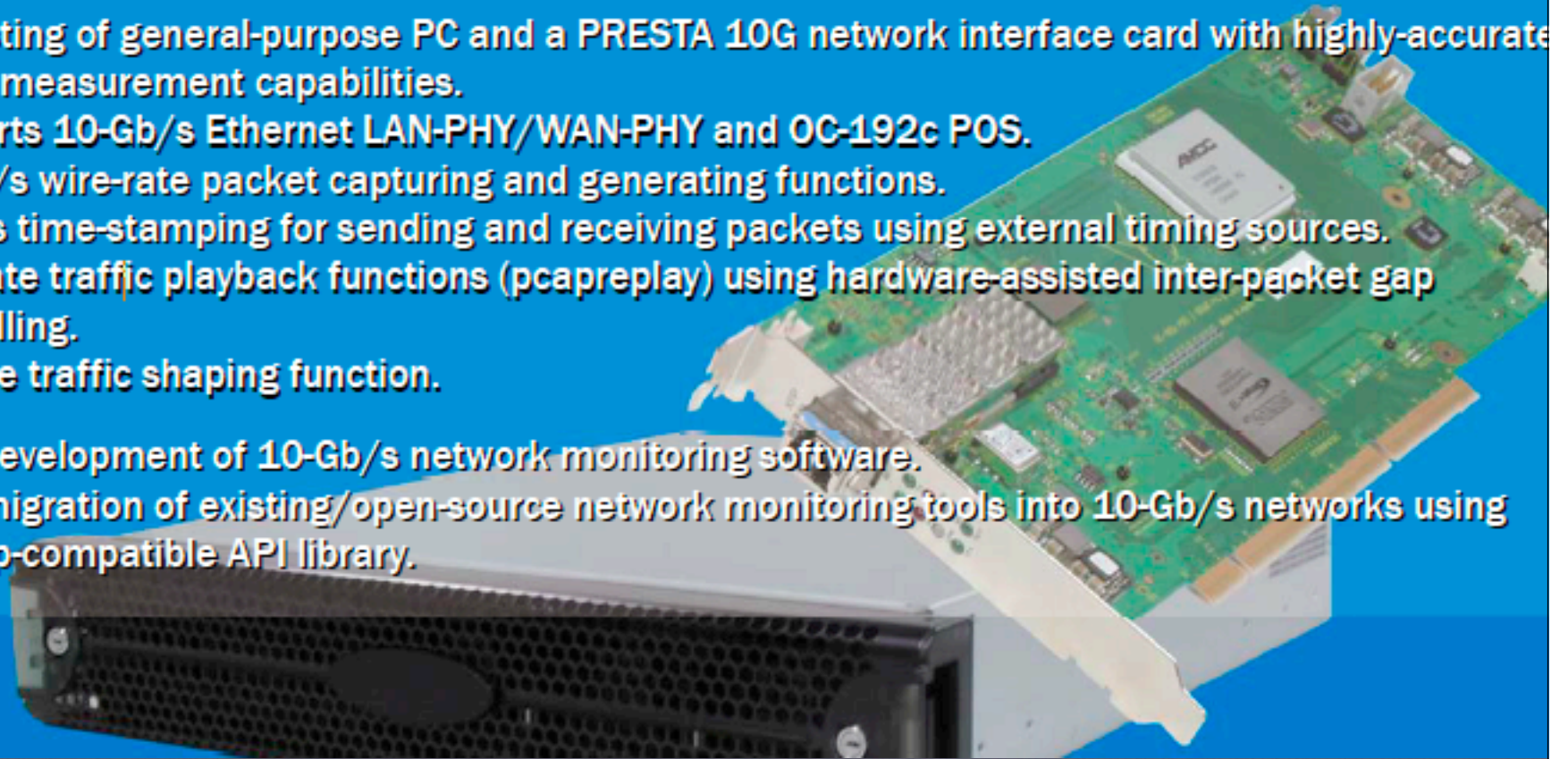


PRESTA 10G Platform:

for high-accuracy 10-Gb/s network monitoring

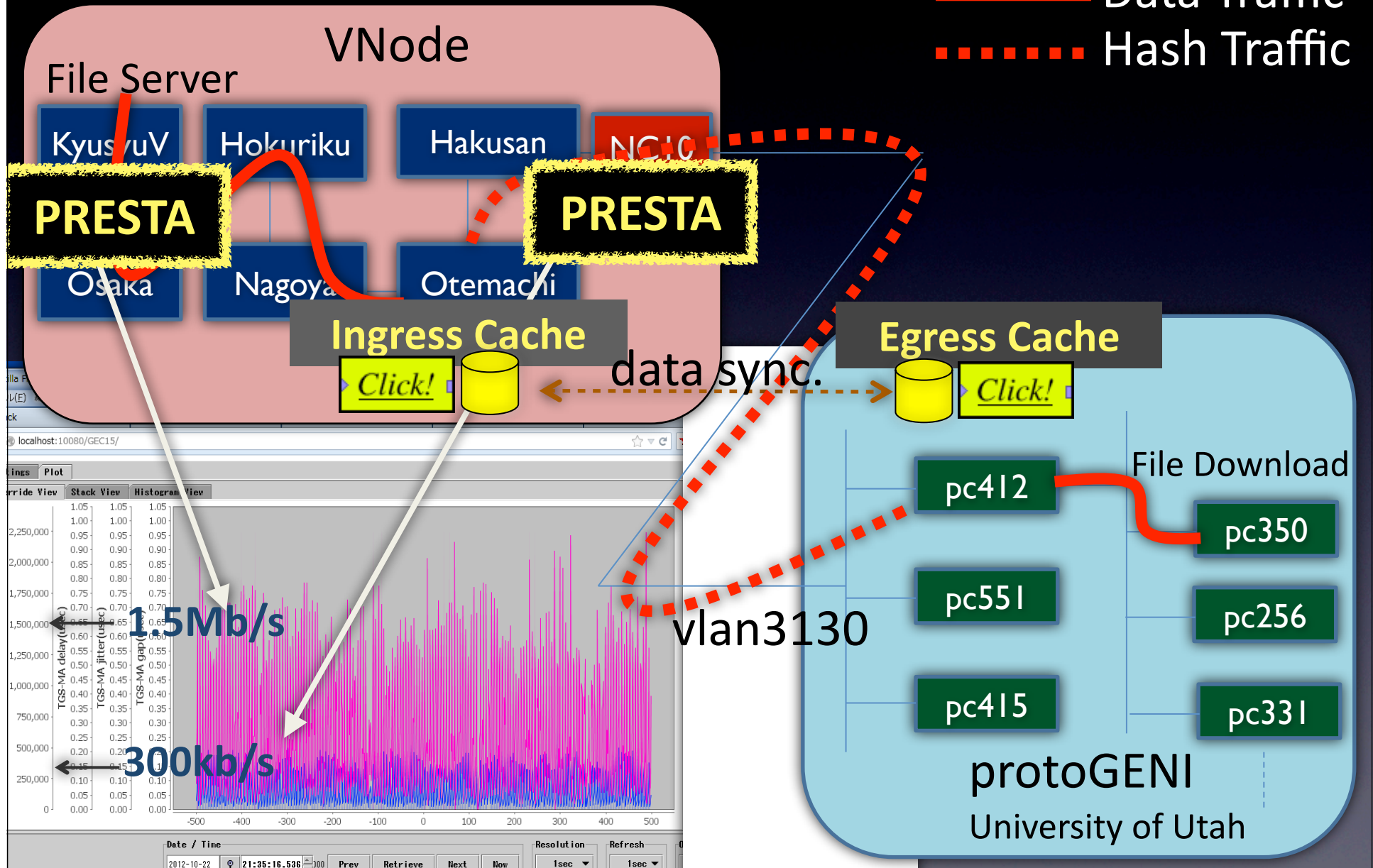
powered by i-Visto technology

- Consisting of general-purpose PC and a PRESTA 10G network interface card with highly-accurate traffic measurement capabilities.
- Supports 10-Gb/s Ethernet LAN-PHY/WAN-PHY and OC-192c POS.
- 10-Gb/s wire-rate packet capturing and generating functions.
- 100-ns time-stamping for sending and receiving packets using external timing sources.
- Accurate traffic playback functions (pcapreplay) using hardware-assisted inter-packet gap controlling.
- Flexible traffic shaping function.
- Easy development of 10-Gb/s network monitoring software.
- Easy migration of existing/open-source network monitoring tools into 10-Gb/s networks using libpcap-compatible API library.



VNode and GENI packet Cache Demo

— Data Traffic
- - - Hash Traffic



Live Demonstration

Mozilla Firefox

ファイル(E) 編集(E) 表示(V) 履歴(S) ブックマーク(B) ツール(I) ヘルプ(H)

Flack x Emulab.Net - Login x Larry Hall (Cygwin... x Slice details for cl... x super market - Go... x GEC15Agenda/We... x iGoogle x http://lo...0/GEC15/ x

localhost:10080/GEC15/ Yahoo! JAPAN

Settings Plot

Override View Stack View Histogram View

PSA-MA bitrate(bps)

Original Traffic

Visible All			Invisible All		
Type	Name	Value	Type	Name	Value
<input checked="" type="checkbox"/>	PS...	HAKUSAN PSA(t...			
<input checked="" type="checkbox"/>	PS...	TENJIN PSA(to...			

Date / Time: 2012-10-24 23:41:53.311 300 Prev Retrieve Next Now

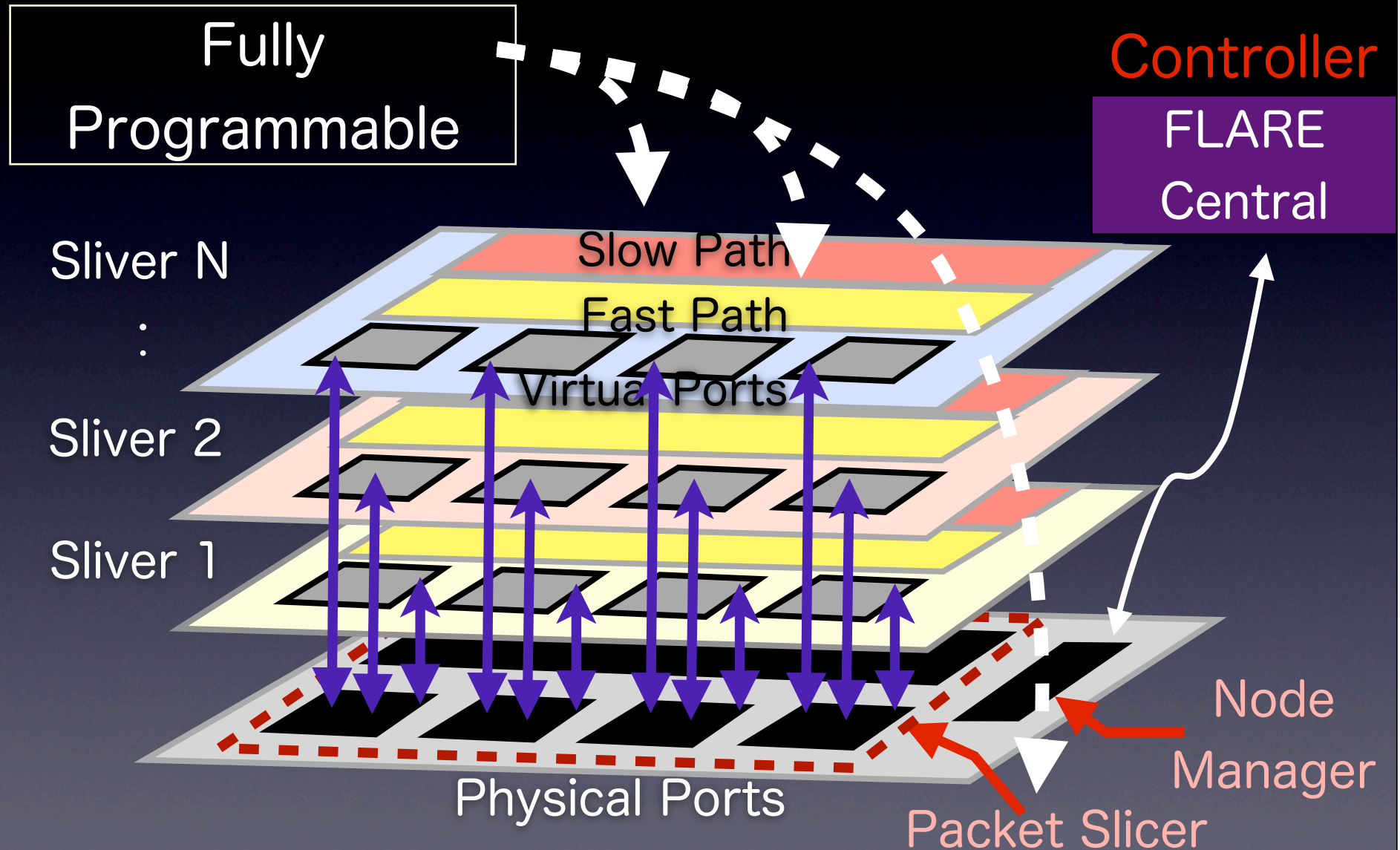
Resolution: 1sec Refresh: 1sec Output: CSV

23:50 2012/10/24

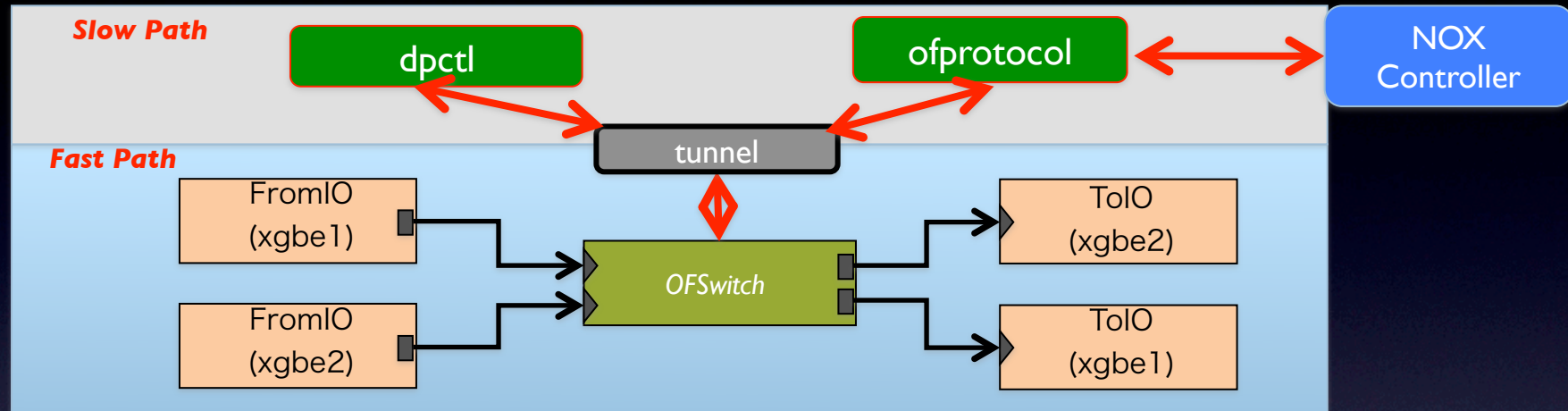
Hash Traffic

FLARE Update

FLARE Architecture



Programming Model

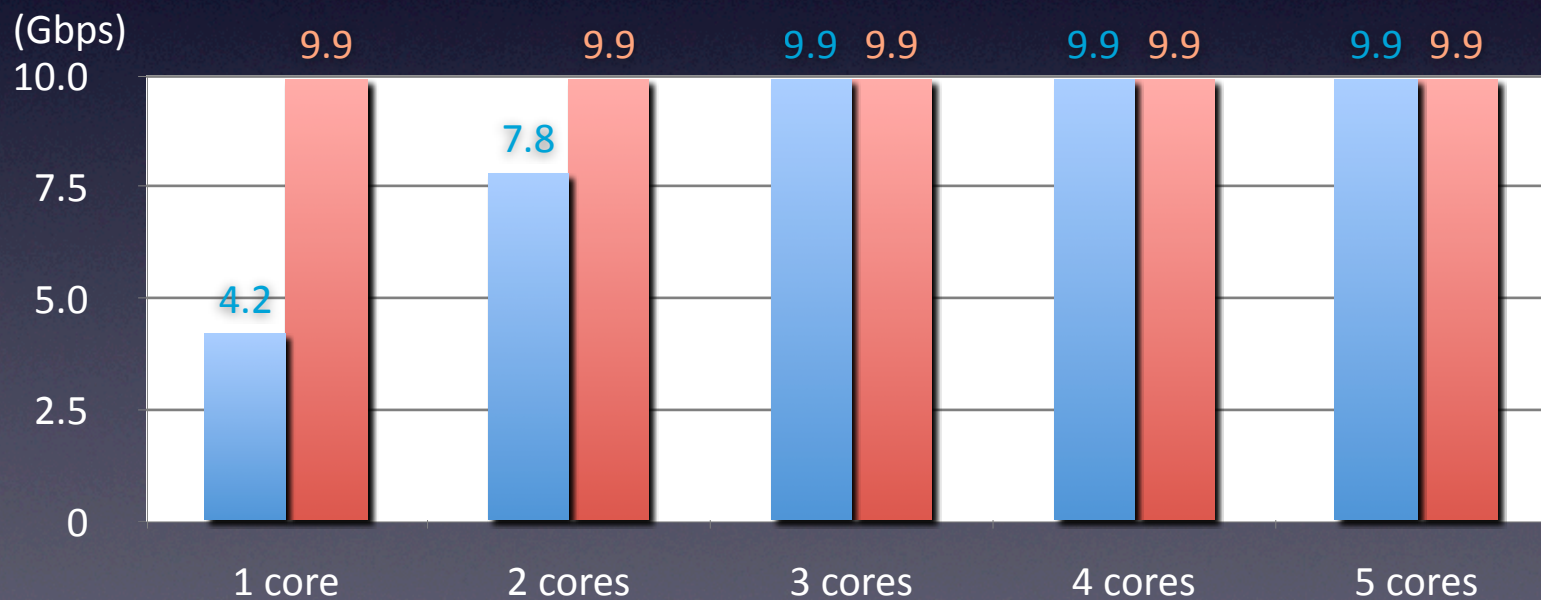
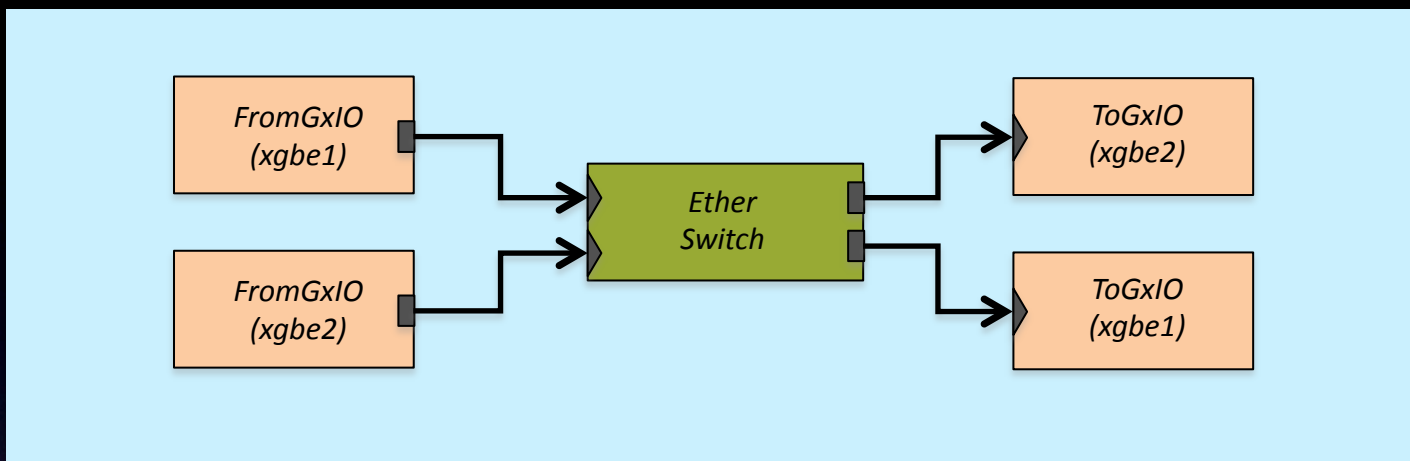


Multi-Threaded Modular Programming

e.g., Click Software Modular Router (multi-threaded)

- Arbitrary switch logic(s) can be implemented in **fast-path, slow-path and slicer sliver** (e.g., OpenFlow switch logic can be modified/refined)

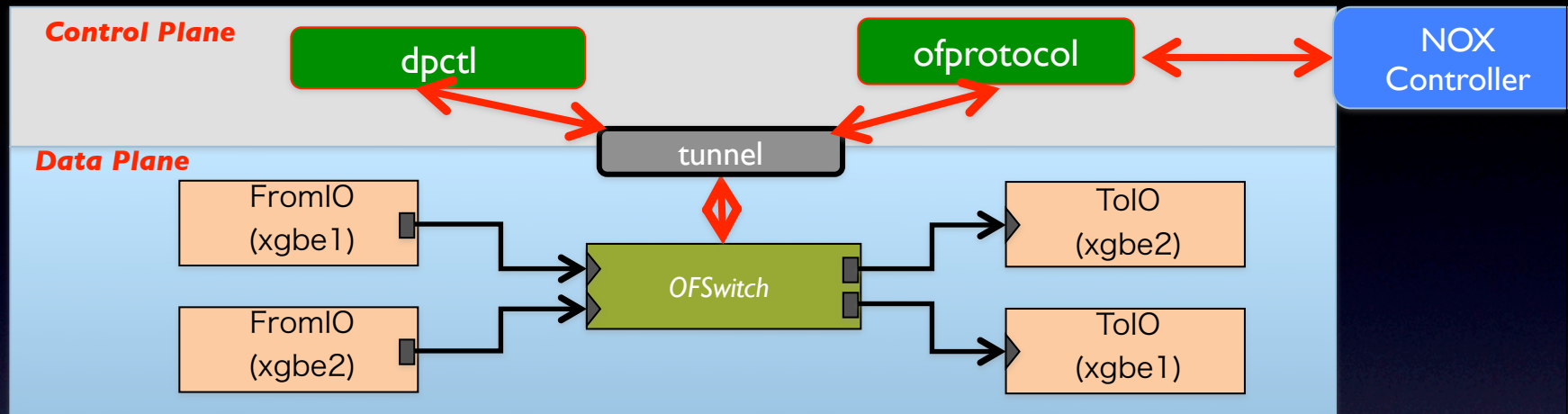
Ethernet Switch



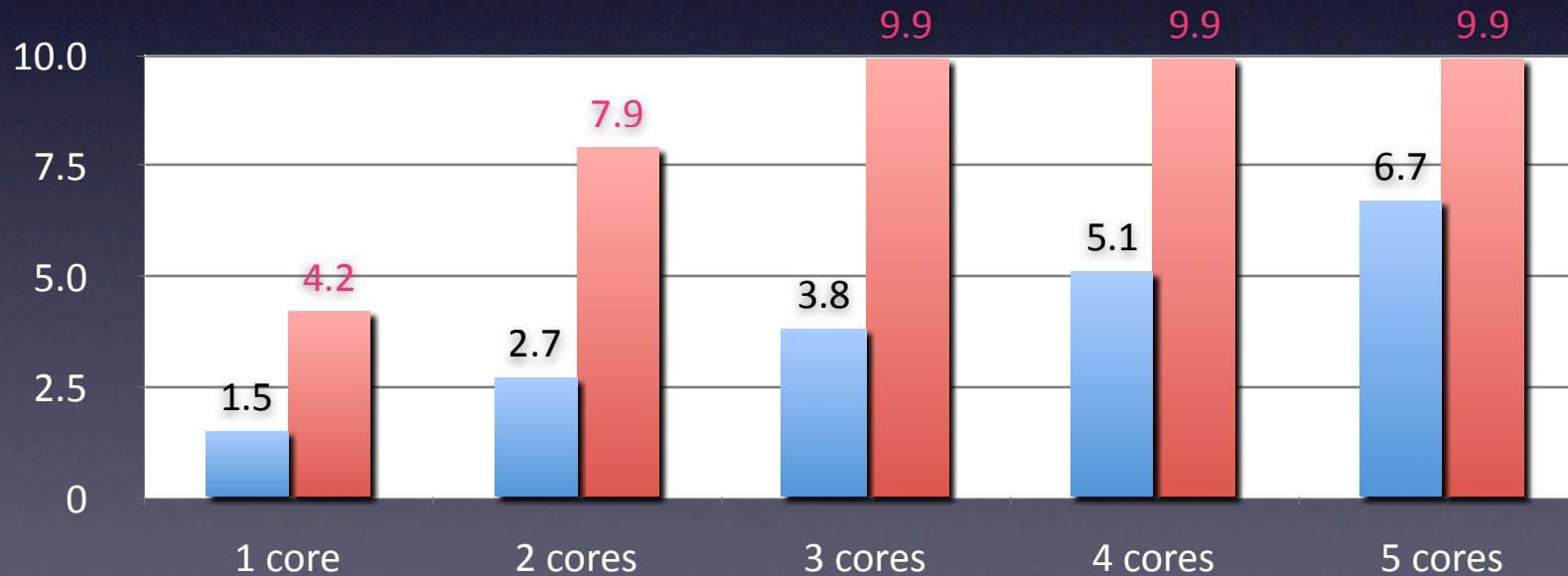
Switching Performance
The University of Tokyo Confidential

■ pkt_size=512B
■ pkt_size=1514B

OpenFlow Switch



(Gbps)



Switching Performance

pkt_size=512B

pkt_size=1514B

Summary

- Data Plane Federation just started
- Control Plane Federation (NC->SEP)
- More Geographical Distribution
- More Applications(Packet Cache, XIA, ...)
- FLARE Switch in ProtoGENI :-)

Credits

- VNode Team (NICT, UTokyo, NTT, Hitachi, KDDI, NEC, Fujitsu)
- PRESTA Team (NTT)
- ProtoGENI Team
- XIA Team
- NICT / JGN-X & KDDI
- Ministry of Internal Affairs and Communications (MIC)
- GENI Project Office
- iCAIR/Starlight
- instaGENI / HP Labs
- UTokyo NakaoLab (FLARE-dev Team)